

# 7 Application Notes



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## 7.1 Overview

The Application Notes elaborate on issues arising from designing this chip into computer systems. The first one, Board Design, covers board design by pin function group. Each section has a simple pin connection diagram, showing different designs where there is more than one way to use these pins.

The On-Board testing section describes how to use the built-in testing functions in SM3110 to isolate motherboard problems without removing the SM3110 from the board.

The Programmable I/O section shows the use of both types of programmable I/O in SM3110 in customizing system designs with unique functions.

The Power-On Configuration section describes the chip configuration that must be set at power up time for SM3110 to function properly on each system type.

## 7.2 Board Design

The board is divided into sections, with each functional pin group having a block diagram as an overall view of display subsystem, including the host interface, reference clock, LVDS interface, LCD panel interface, CRT interface, BIOS ROM interface, TV encoder interface and power-on strapping.

## 7.2.1 Power Supply

The SM3110 uses 3.3V and 2.5V. The 3.3V is only for the I/O pads and should be applied to the power pins marked as VDD\_IO.

2.5V power has been divided into several sections. The first one, VDD\_C, is for the digital core section. This section requires the highest current in the 2.5V section when the chip is in normal operation. The VDD\_R is the 2.5V for embedded memory section. VDD\_P and VDD\_S are 2.5V for digital section of internal PLLs and DLL section, respectively. AVDD\_P, AVDD\_S, and AVDD\_D are 2.5V for analog portion in PLLs, DLL, and DACs, respectively. PCB layout for these different power supplies must be done carefully to prevent noise generated from one section coupling into any other section. A ground layer in the PCB is recommended for the entire display subsystem section.

7.2.2 Block Diagram

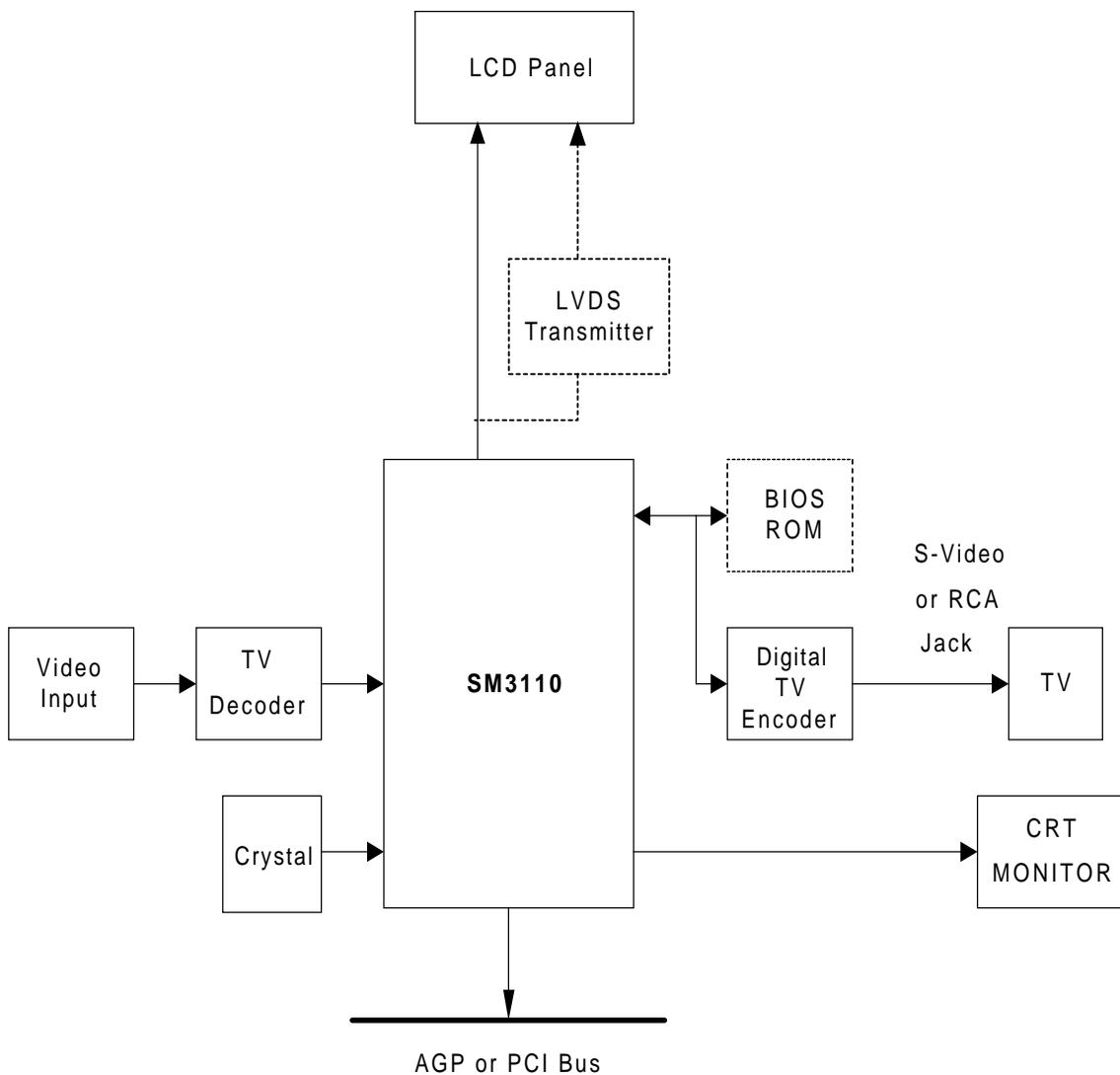
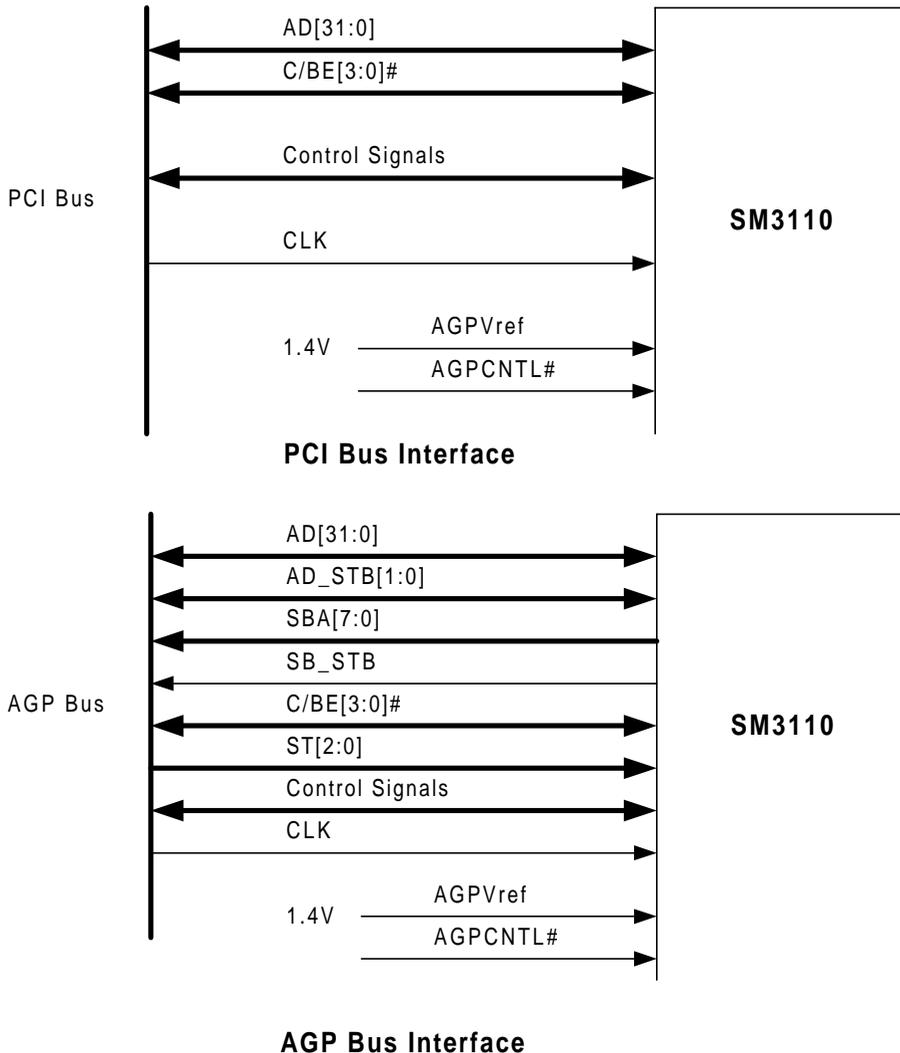


Figure 7-1. SM3110 System Diagram

### 7.2.3 Host Interface

The SM3110 supports either AGP 1X/2X or PCI 66 MHz interface. A power-on strapping pin determines the interface type and must be set correctly for communicating with the CPU. See the Power-On Configuration section for details of strapping options.



**Figure 7-2. SM3110 Interfaces to Host**

The 2X AGP bus uses strobing signals on the receiving side to latch input data at the correct time. The layout of these strobing signals and their corresponding data/address lines must be carefully done to ensure the trace lengths are within specification (see AGP Specification version 2.0 and AGP Platform Design Guide for more detailed layout considerations).

## 7.2.4 Reference Clock

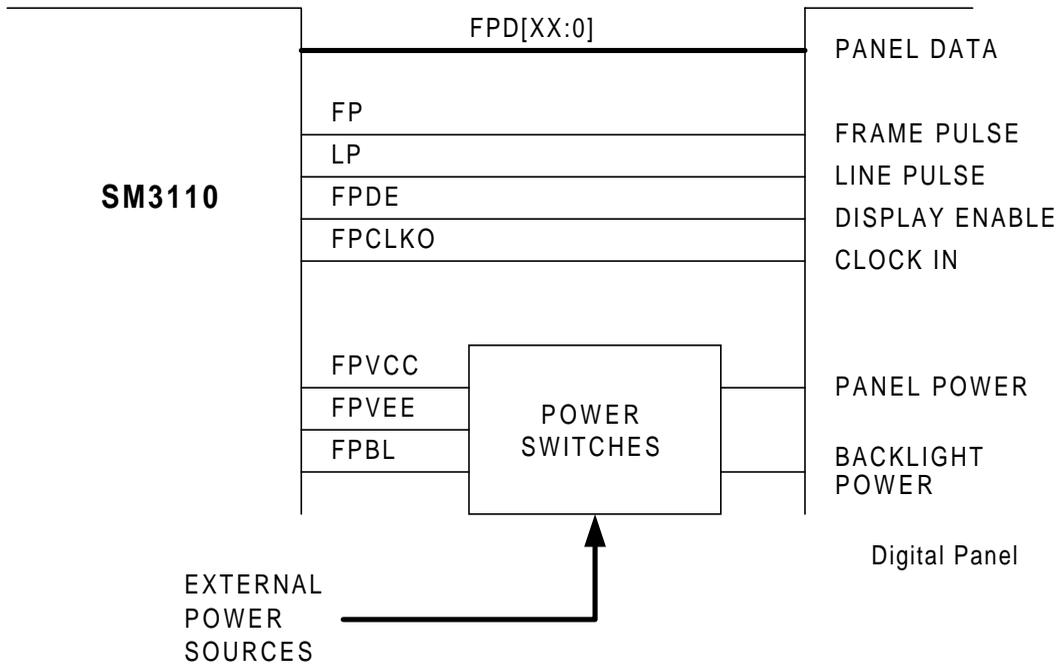
The SM3110 requires a single reference clock input for its internal PLLs. These PLLs can be programmed individually to generate 3 different clocks used by the chip. The typical frequency of this reference clock is 14.31818 MHz. However, it can be any frequency from 2 MHz to 40 MHz. This clock can be from either a crystal (with external resistors and capacitors) or a CMOS level oscillator. Please refer to the drawing below for the usage of these two types of circuit.



**Figure 7-3. Reference Clock Methods**

### 7.2.5 LCD Panel Interface

The SM3110 provides 36 pixel data pins and all other timing and control pins needed to interface with any LCD flat panel. It supports 8-bit, 16-bit, or 12+12-bit DSTN panel. For TFT panel, 9-bit, 12-bit, 18-bit, 24-bit, 9+9-bit, 12+12-bit, and 18+18-bit are supported. The data/pin assignment is listed in Table 7-1.



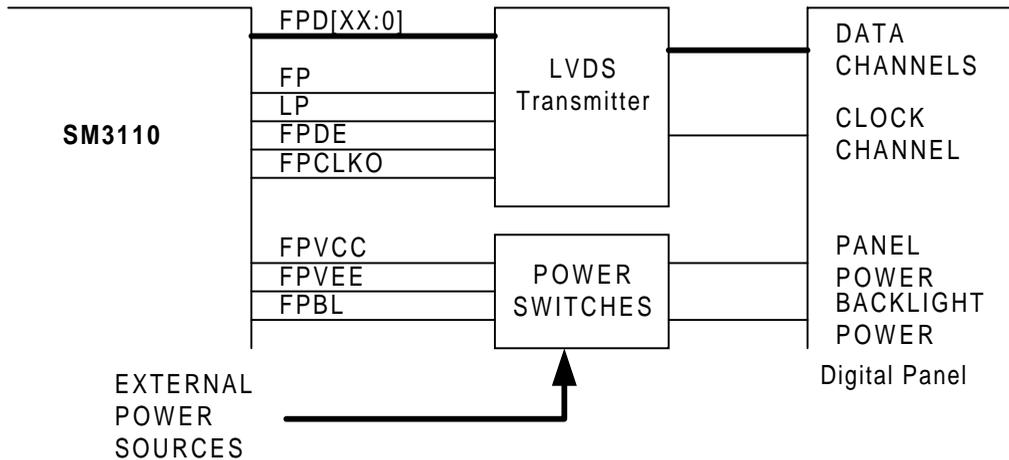
**Figure 7-4. Digital Panel Interface Diagram**

**7.2.6 LVDS Transmitter Interface**

SM3110's 36 pixel data, timing and control pins can interface with any LVDS transmitter(s), which can in turn drive an LCD panel with an LVDS interface.

The SM3110 supports 8-bit, 16-bit, or 12+12-bit DSTN panels as well as 9-bit, 12-bit, 18-bit, 24-bit, 9+9-bit, 12+12-bit and 18+18-bit TFT panels. The data/pin assignment is listed in Table 7-1.

To drive a panel through the LVDS interface, an LVDS transmitter chip is required. A block diagram is provided below for reference.



**Figure 7-5. LVDS Panel Interface**

**Table 7-1. FPD[35:0] Different Panel Type Settings**

Bit per Pixel	TFT									
	Single Pixel				Double Pixel			DSTN		
	9	12	18	24	9+9	12+12	18+18	4+4	8+8	12+12
Pin Name										
FPD0	B0	B0			FB0	FB0	UR1	UR0	UR0	
FPD1	B1	B1			FB1	FB1	UG1	UG0	UG0	
FPD2	B2	B2			FB2	FB2	UB1	UB0	UB0	
FPD3	B3	B3			FB3	FB3	UR2	UR1	LR0	
FPD4	B4	B4			SB0	FB4	LR1	LR0	LG0	
FPD5	G0	B5			SB1	FB5	LG1	LG0	LB0	
FPD6	G1	B6			SB2	SB0	LB1	LB0	UR1	
FPD7	G2	B7			SB3	SB1	LR2	LR1	UG1	
FPD8	G3	G0			FG0	SB2	-	UG1	UB1	
FPD9	G4	G1			FG1	SB3	-	UB1	LR1	
FPD10	G5	G2			FG2	SB4	-	UR2	LG1	
FPD11	R0	G3			FG3	SB5	-	UG2	LB1	
FPD12	R1	G4			SG0	FG0	-	LG1	UR2	
FPD13	R2	G5			SG1	FG1	-	LB1	UG2	
FPD14	R3	G6			SG2	FG2	-	LR2	UB2	
FPD15	R4	G7			SG3	FG3	-	LG2	LR2	
FPD16	-	-	R0		FR0	FG4	-	-	LG2	
FPD17	-	-	R1		FR1	FG5	-	-	LB2	
FPD18	-	-	R2		FR2	SG0	-	-	UR3	
FPD19	-	-	R3		FR3	SG1	-	-	UG3	
FPD20	-	-	R4		SR0	SG2	-	-	UB3	
FPD21	-	-	R5		SR1	SG3	-	-	LR3	
FPD22	-	-	R6		SR2	SG4	-	-	LG3	
FPD23	-	-	R7		SR3	SG5	-	-	LB3	
FPD24	-	-	-	-	--	FR0	-	-	-	
FPD25	-	-	-	-	--	FR1	-	-	-	
FPD26	-	-	-	-	--	FR2	-	-	-	
FPD27	-	-	-	-	--	FR3	-	-	-	
FPD28	-	-	-	-	--	FR4	-	-	-	
FPD29	-	-	-	-	--	FR5	-	-	-	
FPD30	-	-	-	-	--	SR0	-	-	-	
FPD31	-	-	-	-	--	SR1	-	-	-	
FPD32	-	-	-	-	--	SR2	-	-	-	
FPD33	-	-	-	-	--	SR3	-	-	-	
FPD34	-	-	-	-	--	SR4	-	-	-	
FPD35	-	-	-	-	--	SR5	-	-	-	

### 7.2.7 CRT Monitor Interface

The SM3110 uses a standard analog RGB interface to drive a CRT monitor. Two customer I/O pins, CIO[1:0], use the standard DDC2B protocol to communicate with monitor. The output of DACs are designed to drive a 37.5 Ohm load. The optimum loading connection is a 75 Ohm resistor to the ground and a 75 Ohm cable load to the VGA connector. The PCB layout for this section needs to be done carefully, since these analog signals are prone to noise.

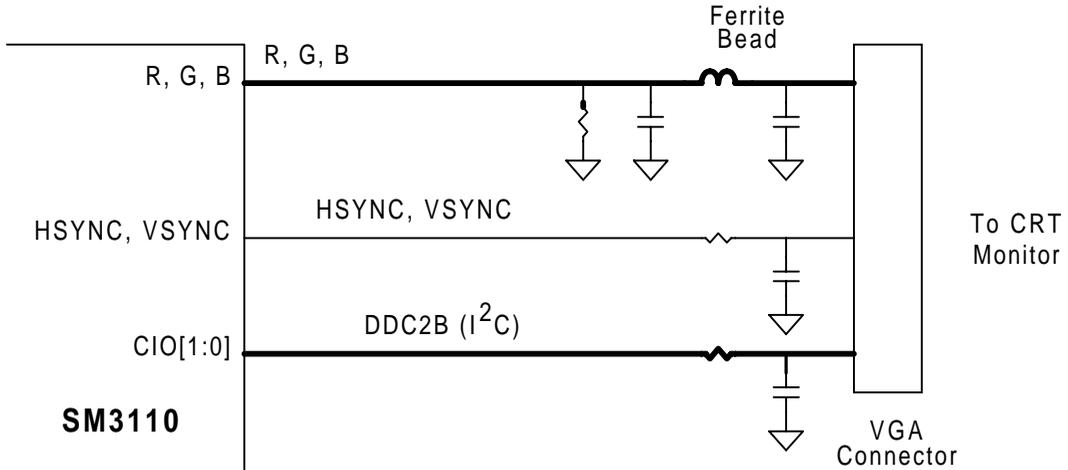
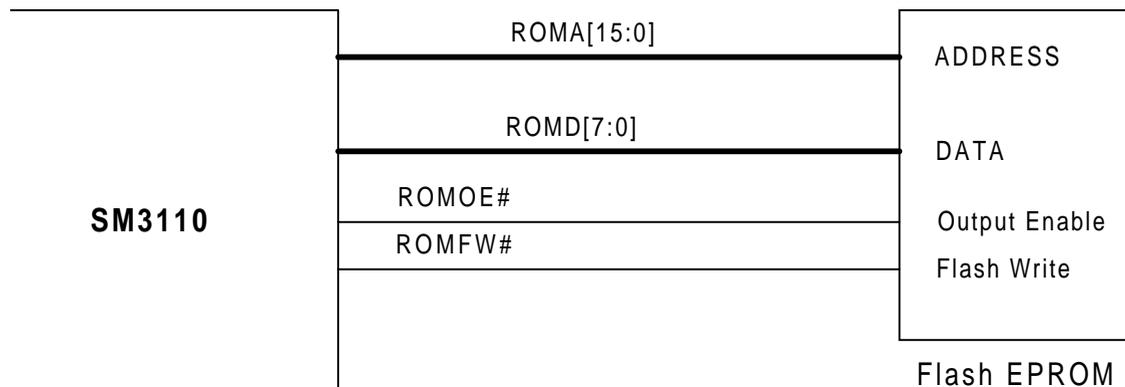


Figure 7-6. CRT Monitor Interface

### 7.2.8 BIOS ROM Interface

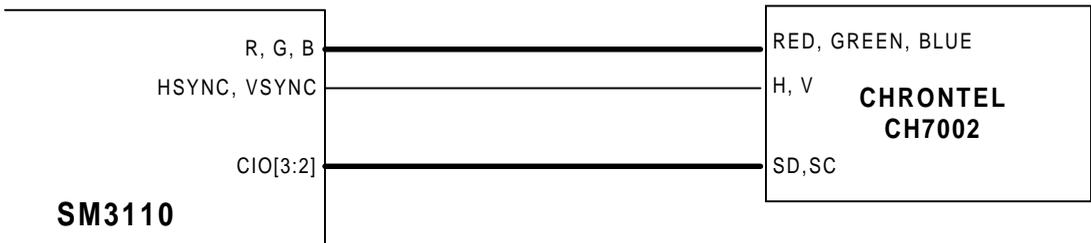
The SM3110 supports external BIOS ROM. The ROM can be EPROM, EEPROM, or flash ROM for easy field update. The ROM size can be either 32 KB or 64 KB, set by a power-on strapping pin.



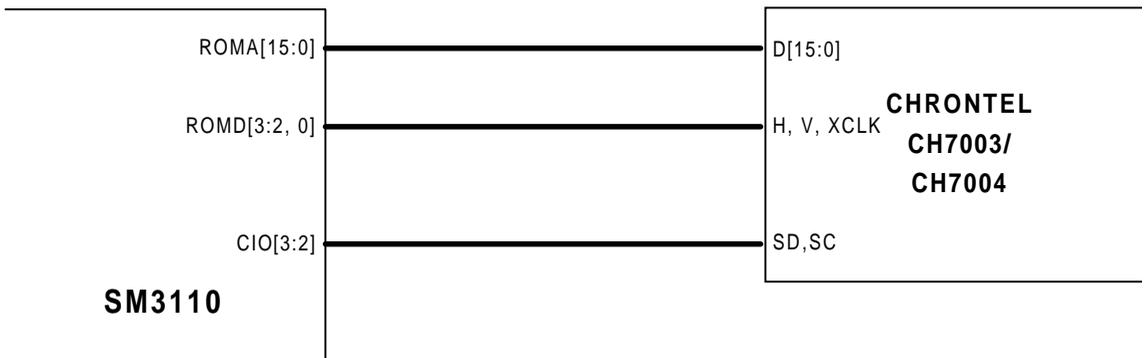
**Figure 7-7. BIOS ROM Interface**

## 7.2.9 Analog and Digital TV Encoder Interfaces

The SM3110 supports both analog and digital types of TV encoders. The analog type receives data from RGB lines in a CRT monitor interface. A typical hook-up is shown in Figure 7-8, using Chrontel’s CH7002 analog encoder. The digital type can use either ROM interface or panel interface. For most applications, the ROM interface is where the external TV encoder chip connects. The ROM interface provides 16 bits of RGB data and timing signals (HSYNC, VSYNC and DCLK) for the encoder chip. Any TV encoder chip that can accept 16-bit RGB non-interlace signal can be used. A Chrontel CH7003/7004 is used in the sample design illustrated in Figure 7-9. Please refer to the Alternate Output Function portion of the Datasheet and the Register Summary for detailed signal assignment and register controls.



**Figure 7-8. Analog TV Encoder Interface**



**Figure 7-9. Digital TV Encoder Interface**

### 7.2.10 TV Decoder Interface

The SM3110 supports an external TV decoder chip to provide live video window and video capture functions. The interface can connect to either standard PCMCIA ZV Port or Philips' SA7111/7112 (or compatible) TV decoder chip. The connection is straightforward, and the control to the external TV decoder is through the I<sup>2</sup>C interface.

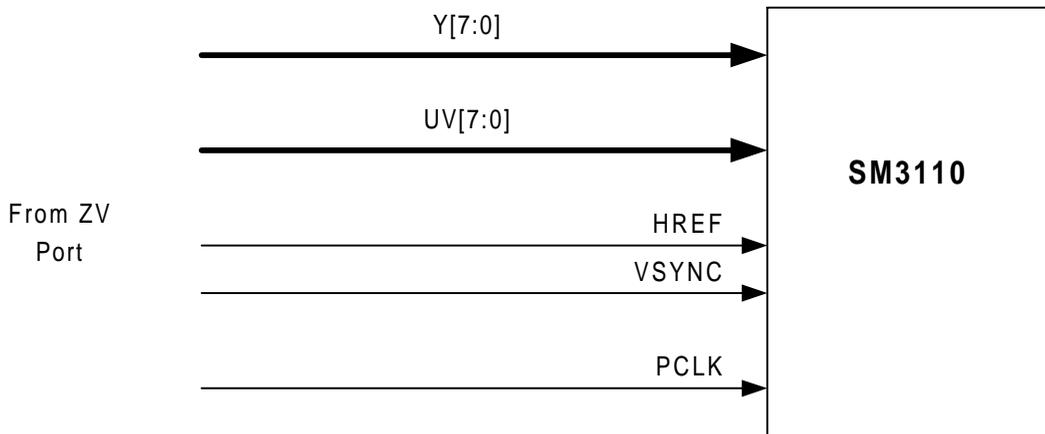


Figure 7-10. ZV Port-TV Decoder Interface

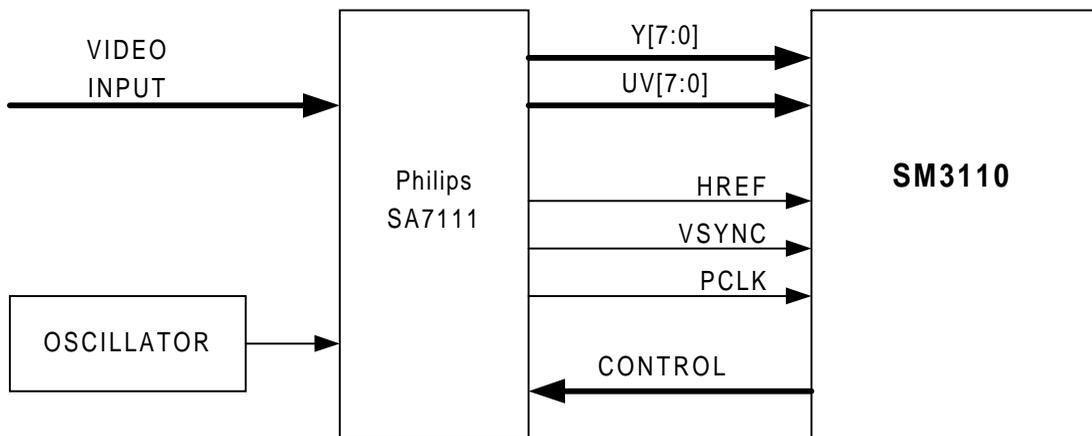


Figure 7-11. Philips TV Decoder Interface

## 7.3 Power-On Strapping

Eight pins in the ROM interface are also used as Power-On Strapping pins in setting SM3110 configuration within a particular system design. One of these pins is designed to control AGP/PCI interface selection, one is designed to select 32K/64K ROM size, two are for debugging use and four are for customer defined functions, such as panel type. These pins have an internal pull-up resistor and therefore default to “HIGH” without any external component. Refer to the alternate pin function section in the Datasheet.

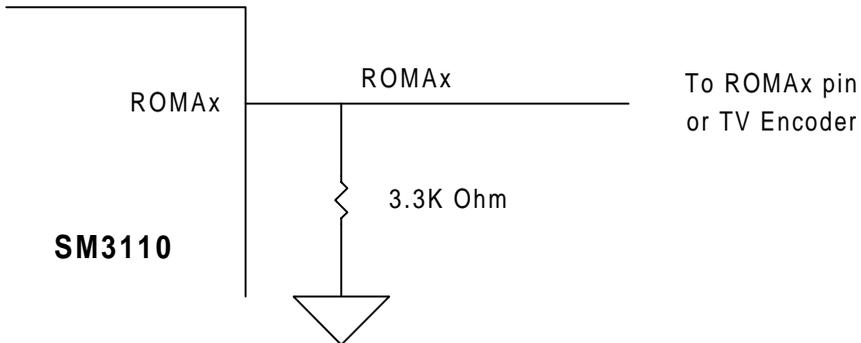


Figure 7-12. Power-on Strapping

### 7.3.1 Power-on Strapping Pins

Ball No.	Primary Pin Function	Configuration Function		Note
		Default	w/Pull-down Resistor	
C23	ROMA8	CONFIG[0]		User Defined
D22	ROMA9	CONFIG[1]		User Defined
E21	ROMA10	CONFIG[2]		User Defined
F20	ROMA11	CONFIG[3]		User Defined
D23	ROMA12	32K ROM	64K ROM	
E22	ROMA13	Reserved		
F21	ROMA14	Reserved		
E23	ROMA15	AGP Host Interface	PCI Host Interface	

## 7.3.2 Strapping Method

During reset time, RST# is low and ROMA8 through ROMA15 are forced to be input pins. Each pin has an internal pull-up resistor to set the pin value high, if no external pull-down resistor or other driving force is used to bring the signal level to low. At the trailing edge of reset (RST# changes from low to high), the values of these pins are latched into registers where they can be read by software. Because these functions are set according to the hardware configuration of the board, changes are not allowed. If they are somehow changed, the chip and board may not function properly.

### 7.3.2.1 External Pull Down Resistor

Each pin has internal pull-up resistor to default the pin value to high. Some pins have inverters between pin and register bit and so the default value in the register is inverted from the default value at the pin. Please refer to the **Registers** section below for the default value of each bit. If default value is the right setup for the bit, no external resistor is required. However, if the other value is needed, a 3.3K Ohm resistor should be added between the corresponding pin and ground.

### 7.3.2.2 Registers

The register bits that control these configuration functions are listed below.

<i>Offset</i>	<i>Field</i>	<i>Access</i>	<i>Function</i>
+4C0H	7:00	R/O	<b>Configuration Strapping</b>
	<i>Bits</i>		<i>Field</i>
	07		AGP or PCI Select.
			<i>External Pull-down Resistor</i> <i>Value</i> <i>Semantics</i>
			No (default)      0      PCI. Default.
			Yes      1      AGP
	<i>Bits</i>		<i>Field</i>
	06:05		Reserved (must be zero))
	<i>bits</i>		<i>field</i>
	04		ROM Select (32K or 64K).
			<i>External Pull-down Resistor</i> <i>Value</i> <i>Semantics</i>
			No (default)      0      32K
			Yes      1      64K
	<i>Bits</i>		<i>Field</i>
	03:00		User Defined
			<i>External Pull-down Resistor</i> <i>Value</i> <i>Semantics</i>
			Yes      0      User Defined
			No (default)      1      User Defined

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## 7.3.2.3 *Strapping Pin Functions*

### **Host Interface**

This pin determines what type of host interface the chip is talking to. The default is PCI.

### **ROM Size**

This pin sets the external BIOS ROM size. The default is 32 KB. With a pull-down resistor, the size is set to 64 KB (this is only for the external BIOS ROM that interfaces to the chip through the chip's ROM interface).

### **User Defined**

These pins are for user defined functions, such as panel type. Both the driver and the BIOS can read the register to determine what setting the system requires through any or all of these four pins.

### **Reserved**

There are two reserved power-on strapping pins. These pins must NOT have external pull-down resistors.

## 7.4 Board-level Testing

The SM3110 currently implements two board-level testing modes: Connectivity Test Mode and Tri-State Mode.

### 7.4.1 Test Mode Control Pins

There are five pins that control test modes. The TEST# pin should be left unconnected in normal operation, since an internal pull-up sets the chip in normal operation mode. To enter test mode, this pin must be driven to low from outside the chip and maintained at that level during test operation.

The four other pins are used to select different test modes. These four pins have normal functions when TEST# is not connected. The table below lists the pin name (in normal mode and test mode), pin number and setting required for each different test mode.

**Table 7-2. Test Mode Control Pins**

Pin Name	Pin No.	C15	C2	B1	A1	D4	Test Mode
	Normal	TEST#	FPD28	FPD27	FPD26	FPD25	
	Test	TEST#	TEST3	TEST2	TEST1	TEST0	
Setting		1	-	-	-	-	Normal Operation
		0	0	0	0	0	Reserved
		0	0	0	0	1	Reserved
		0	0	0	1	0	Reserved
		0	0	0	1	1	Reserved
		0	0	1	X	X	Reserved
		0	1	0	X	X	Reserved
		0	1	1	0	X	Reserved
		0	1	1	1	0	IO Connectivity Test
		0	1	1	1	1	Tri-State All Outputs

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## 7.4.2 Test Modes

The I/O Connectivity Test Mode helps in identifying soldering problems on the PCB. In this mode, all digital pins except the TEST# pin and the TEST[3:0] pins are arranged to connect to either input or output of NAND gate array.

To perform this test, set TEST[3:0] to 0xE and apply logical highs to all input pins. All the output pins should then be at logical low. Any output that is not in the correct logic state indicates one of its inputs is either open or shorted to logic low. Next, toggle one input at a time from logic high to logic low and back to logic high; the corresponding output must change from logic low to logic high and back to logic low. All other outputs must stay at logic low. If the corresponding output does not change state, the input pin is open. If another output changes states with the corresponding output, one of its inputs is shorted to this input.

The Tri-State Test Mode isolates the chip from the board during the debugging of other board components. Set TEST[3:0] to 0xF to force all output drivers in output pins and bi-directional pins into tri-state mode.

The connection map is listed below, followed by tables of untested pins and unused pins.

Input		Output	
Pin	Sig. Name	Pin	Sig. Name
Y4	INTA#	H22	IOTST7
AC2	REQ#		
AC4	RBF#		
AC6	SB_STB		
Y6	SBA1	AC1	CLK
AA8	SBA7		
AC8	AD31		
AA9	AD28		
Y8	SBA5	AA4	RST#
AB10	AD27		
Y11	AD24		
Y13	AD22		
AB6	SBA2	AC3	ST0
Y9	AD30		
AC9	AD29		
AA12	C/BE3#		
AB2	CLKRUN#	Y5	GNT#
AC5	SBA0		
Y7	SBA3		
AC7	SBA4		
AB8	SBA6	AB4	ST2
AC10	AD25		
AB12	AD23		
Y15	AD16		
Y10	AD26	AA5	ST1
AC11	AD_STB1		
AA13	AD20		
AC13	AD19		

Input		Output	
Pin	Sig. Name	Pin	Sig. Name
AC12	AD21	AA11	IDSEL
Y14	AD18		
AC14	C/BE2#		
AA16	STOP#		
AB14	AD17	AC19	M66EN
Y16	TRDY#		
AB16	DEVSEL#		
AC18	AD10		
AA15	FRAME#	F23	IOTST1
AC16	C/BE1#		
Y19	AD13		
AB19	AD8		
AC15	IRDY#	G23	IOTST2
AC17	AD14		
AA19	AD11		
Y23	AD4		
AA17	PAR	G22	IOTST3
AA20	C/BE0#		
AC22	AD5		
AA23	AD2		
AB18	AD12	G21	IOTST4
AC21	AD7		
AB23	AD0		
Y18	AD15	G20	IOTST5
AB22	AD3		
Y21	AD6		
AC20	AD_STB0	H23	IOTST6
Y20	AD9		
AC23	AD1		

## Application Notes

Input		Output	
Pin	Sig. Name	Pin	Sig. Name
K22	CIO6	H20	IOTST8
K20	CIO4		
R3	CIO1		
U2	HSYNC		
E23	ROMA15	J23	MCLKOUT
E21	ROMA10		
C23	ROMA8		
E22	ROMA13	J21	SCLKOUT
F20	ROMA11		
L21	ZVPCLK		
A23	ROMA4		
F21	ROMA14	J20	PCLKOUT
D23	ROMA12		
B23	ROMA5		
A21	ROMA1		
D22	ROMA9	T20	ZVVSYNC
E20	ROMA7		
A22	ROMA3		
C20	ROMD7		
C22	ROMA6	T21	ZVHREF
D20	ROMA2		
A20	ROMD6		
D18	ROMD3		
B21	ROMA0	T23	ZVY7
D19	ROMD5		
A18	ROMD2		
D16	ROMOE#		
A19	ROMD4	R20	ZVY6
D17	ROMD1		
B16	ROMXR#		

Input		Output	
Pin	Sig. Name	Pin	Sig. Name
D14	FPDE		
A17	ROMD0	R21	ZVY5
D15	ROMFW#		
A15	FPBL		
A13	LP		
A16	ROMWR#	R22	ZVY4
A14	FP		
D12	FPVEE		
A12	FPD1		
B13	FPVCC	R23	ZVY3
D13	FPCLKO		
A11	FPD3		
A9	FPD9		
C12	FPD0	P20	ZVY2
D10	FPD4		
A10	FPD6		
A8	FPD11		
D11	FPD2	P22	ZVY1
C9	FPD8		
D7	FPD12		
A7	FPD14		
B10	FPD5	P23	ZVY0
D8	FPD10		
B7	FPD13		
D6	FPD15		
C6	FPD16	N20	ZVUV7
A4	FPD19		
C4	FPD23		
D1	FPD31		
D9	FPD7	N21	ZVUV6

Input		Output	
Pin	Sig. Name	Pin	Sig. Name
A6	FPD17		
A3	FPD21		
D2	FPD30		
A5	FPD18	N23	ZVUV5
D5	FPD22		
C1	FPD29		
E2	FPD34		
B4	FPD20	M20	ZVUV4
A2	FPD24		
E4	FPD32		
F1	FPD38		
E3	FPD33	M21	ZVUV3
E1	FPD35		
G4	FPD39		
H2	FPD44		
F4	FPD36	M22	ZVUV2
H4	FPD42		
H1	FPD45		
L22	CIO2		
F3	FPD37	M23	ZVUV1
G1	FPD41		
H3	FPD43		
K23	CIO7		
G2	FPD40	L20	ZVUV0
J4	FPD46		
J2	FPD47		
T4	BLANK#		
K21	CIO5	U23	ZVCREF
L23	CIO3		
R4	CIO0		
U1	VSYNC		

## Application Notes

Untested Pins	
T1	DCLK
U4	RSET
V1	COMP
V4	RED
V3	GREEN
W1	BLUE
AA1	AGPCNTL#
Y22	AGPVref
W21	XCLK1
W20	XCLK0
C15	TEST#
D4	FPD25
A1	FPD26
B1	FPD27
C2	FPD28

Unused Pins	
AA7	Reserved17
AB21	Reserved21
J1	Reserved1
K1	Reserved4
K3	Reserved3
K4	Reserved2
L1	Reserved7
L2	Reserved6
L4	Reserved5
M1	Reserved8
M3	Reserved9
M4	Reserved10
N1	Reserved11
N2	Reserved12
N4	Reserved13
P1	Reserved14
P3	Reserved15
P4	Reserved16
R1	VREFIN
R2	VREFOUT
Y12	Reserved19
Y17	Reserved20

## 7.5 Programmable (Peripheral) I/O

There are two types of programmable I/O in the SM3110. The first is through eight 'customer' I/O pins and the second type is peripheral I/O which uses the ROM interface address and data pins plus two command pins.

### 7.5.1 Customer I/O

The eight customer I/O pins are controlled directly by register bits. These pins can be individually programmed to be either input or output pins. If set to be input, the value at the pin (either one (high) or zero (low)) can be read from corresponding register bit by software through the normal register read methods. If set as output, writing to the corresponding register bit will set the output value at the pin.

#### 7.5.1.1 Customer Pins

Four of the eight pins are used for I<sup>2</sup>C function to support DDC2B for CRT monitor and to provide TV encoder/decoder control. The remaining four pins are for customer-definable functions. They can be customized for each design and could control a number of different circuits on the system. Please refer to the table below for the pin number and its corresponding signal name.

**Table 7-3. Customer I/O Pins**

Pin	Signal Name	Description
K23	CIO7	User programmer input/output [7]
K22	CIO6	User programmer input/output [6]
K21	CIO5	User programmer input/output [5]
K20	CIO4	User programmer input/output [4]
L23	CIO3	User programmer input/output [3]/I <sup>2</sup> C Data Line
L22	CIO2	User programmer input/output [2]/I <sup>2</sup> C Clock Line
R3	CIO1	User programmer input/output [1]/DDC2B Data Line
R4	CIO0	User programmer input/output [0]/DDC2B Clock Line

## 7.5.1.2 Customer Registers

There are three bytes of register to control these pins. The first one is READ-ONLY and is for getting signal level of pins. The second one is for output level at pin. The third one is to control direction of pin. The offset and function of each register bit is described in following tables.

### CIO Input

<i>Offset</i>	<i>Field</i>	<i>Access</i>	<i>Function</i>
<b>+410H</b>	<b>07:00</b>	<b>R/O</b>	<b>Configurable Input Port</b>
	<i>Bits</i>	<i>Field</i>	
	07:00	Input.	
		<i>Value</i>	<i>Semantics</i>
		0	Level at pin input is low.
		1	Level at pin input is high.

### CIO Output

<i>Offset</i>	<i>Field</i>	<i>Access</i>	<i>Function</i>
<b>+411H</b>	<b>07:00</b>	<b>R/W</b>	<b>Configurable Output Port</b>
	<i>Bits</i>	<i>Field</i>	
	07:00	Output. Write	
		<i>Value</i>	<i>Semantics</i>
		0	Level to pin output is low.
		1	Level to pin output is high.
	<i>Bits</i>	<i>Field</i>	
	07:00	Output. Read	
		<i>Value</i>	<i>Semantics</i>
		0	Level last written to pin output is low.
		1	Level last written to pin output is high.

### CIO Control

<i>Offset</i>	<i>Field</i>	<i>Access</i>	<i>Function</i>
<b>+412H</b>	<b>07:00</b>	<b>R/W</b>	<b>Configurable Control Port</b>
	<i>Bits</i>	<i>Field</i>	
	07:00	Enable. <i>Default</i> is FFH, all bits disabled.	
		<i>Value</i>	<i>Semantics</i>
		0	Output is enabled and pulled low.
		1	Output is disabled.

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## 7.5.2 Peripheral I/O

The peripheral I/O shares ROM interface pins with other functions. Bit 3 and 2 in register offset 400H control the function of these pins. To use this function, both bits should be set to 0 for ROM function. Peripheral I/O functions share the ROMA[15:0] and ROMD[7:0] pins with the ROM interface but use different address range and command pins.

Peripheral I/O occupies a 64KB address range, offset 1FE0000H to 1FEFFFFH, in each 32MB of memory space within total 128MB of memory space reserved. The lower 16-bit of address will output to ROMA[15:0] pins during the command cycle. For read operation, ROMXR# will be asserted and data at ROMD[7:0] pins will be read. For write operation, ROMXW# will be asserted and data will place at ROMD[7:0] pins. Refer to the SM3110 Datasheet for specific timing values.

## 7.5.2.1 Peripheral I/O Pins

Pin	Signal Name	POWERUP Configuration	Alternate Function	Description
E20, C22, B23, A23, A22, D20, A21, B21	ROMA[7:0]		VDO[7:0]	ROM Address [7:0]/ Digital Data[7:0] for TV/TMDS/LVDS Encoder
C23	ROMA8	CONFIG[0]	VDO8	ROM Address [8]/ Digital Data[8] for TV/TMDS/LVDS Encoder
D22	ROMA9	CONFIG[1]	VDO9	ROM Address [9]/ Digital Data[9] for TV/TMDS/LVDS Encoder
E21	ROMA10	CONFIG[2]	VDO10	ROM Address [10]/ Digital Data[10] for TV/TMDS/LVDS Encoder
F20	ROMA11	CONFIG[3]	VDO11	ROM Address [11]/ Digital Data[11] for TV/TMDS/LVDS Encoder
D23	ROMA12	32K/64K ROM	VDO12	ROM Address [12]/ Digital Data[12] for TV/TMDS/LVDS Encoder
E22	ROMA13	INT/EXT PLL	VDO13	ROM Address [13]/ Digital Data[13] for TV/TMDS/LVDS Encoder
F21	ROMA14	INT/EXT SCLK	VDO14	ROM Address [14]/ Digital Data[14] for TV/TMDS/LVDS Encoder
E23	ROMA15	AGP/PCI	VDO15	ROM Address [15]/ Digital Data[15] for TV/TMDS/LVDS Encoder
C20, A20, D19, A19	ROMD[7:4]			ROM Data [7:4]
D18	ROMD3		HSYNC2	ROM Data [3]/ HSYNC for TV/TMDS/LVDS Encoder
A18	ROMD2		VSYNC2	ROM Data [2]/ VSYNC for TV/TMDS/LVDS Encoder
D17	ROMD1		DCLK2	ROM Data [1]/ DCLK for TV/TMDS/LVDS Encoder
A17	ROMD0		BLANK2#	ROM Data [0]/ BLANK# for TV/TMDS/LVDS Encoder
D15	ROMFW#			Flash ROM Flash Write Command
D16	ROMOE#			ROM Output Enable
A16	ROMWR#			Peripheral I/O Write Command
B16	ROMXR#			Peripheral I/O Read Command

## 7.5.2.2 Peripheral I/O Registers

There are six register bits which control these pins: bits [3:2] controls pin function, bits [6:4] control the command pulse width and bit 7 controls the address setup time (bits [1:0] are not part of this function). The details are shown below:

Offset	Field	Access	Function
+400H	07:00	R/W	Peripheral I/O Port Configuration
	Bits	Field	
	07	Address Setup.	
		Value	Semantics
		0	2 clocks. <i>Default.</i>
		1	1 clock.
	Bits	Field	
	06:04	Strobe Width.	
		Value	Semantics
		0	12 clocks. <i>Default.</i>
		1-7	<i>value</i> +4 clocks.
	Bits	Field	
	03:02	ROM port configuration	
		Value	Semantics
		11	Display 0
		10	Display 1
		01	<i>Reserved.</i>
		00	ROM
	01:00	LCD Port Configuration.	
		Value	Semantics
		11	Display 0
		10	Display 1
		01	<i>Reserved.</i>
		00	LCD

Register bits [7:4] of offset 400H control the timing. Bit 7 selects address setup time, either at the default of two system clocks (SCLK) or only one system clock. ROMXR# and ROMXW# strobes (commands) pulse width is set by bits [6:4]. The pulse width is the value in these bits plus 4 system clocks (total range from 5 to 12 system clocks), where 000 in these bits is the default and is treated as 8 to get a total of 12 system clocks of pulse width. The address hold time is fixed at one system clock.

Bit value in 6:4	Clock Value of Bits 6:4	Width of address strobe in System Clocks
000 (default)	8	12
001	1	5
010	2	6
011	3	7
100	4	8
101	5	9
110	6	10
111	7	11

