

65550/554/555 & 69000

**HiQVideo™ Series
Application Note Book**

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Revision History

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Chapter 1

General Interfacing Concerns

Configuring the Graphics Controller for 3V Operation

The graphics controller is optimized for 3V operation, although the part can tolerate 5V signals from the PCI bus and other external interfaces. This document points out the impacts of this feature on the PC board layout and explains some of the concerns that board designers might have.

The 65550 is a fully 5V-tolerant part but can be configured to run as a 3.3V part. Therefore, all VCCs for the graphics controller are 3.3V. These VCCs include AVCC, BVCC, IVCC, and VVCC. Therefore, all output signal levels are 3.3V with VOL rated at 0.5V and VOH rated at 0.7xVCC. All input and bi-directional I/O pads are designed to be 5.0V-tolerant, and the output signals may have external pull-up resistors to 5.0V.

The 65554 is a fully 5V-tolerant part but can be configured to run as a 3.3V part. Therefore, all VCCs for the graphics controller are 3.3V or 5 V. These VCCs include AVCC, BVCC, DVCC, MVCC, PVCC, SVCC and VVCC. Therefore, all output signal levels are 3.3V or 5V with VOL rated at 0.5V and VOH rated at 0.7xVCC. All input and bi-directional I/O pads are designed to be 5.0V-tolerant, and the output signals may have external pull-up resistors to 5.0V.

The 65555 is not a fully 5V-tolerant part, since the core logic must be run at 3.3V per the data sheet. However, all VCCs for the graphics controller are 3.3V. These VCCs include AVCC, BVCC, DVCC, MVCC, PVCC, SVCC and VVCC. Therefore, all output signal levels are 3.3V with VOL rated at 0.5V and VOH rated at 0.7xVCC. All input and bi-directional I/O pads are designed to be 5.0V-tolerant, and the output signals may have external pull-up resistors to 5.0V.

The 69000 is not a fully 5V-tolerant part, since the core logic must be run at 3.3V per the data sheet. However, all VCCs for the graphics controller are 3.3V or 5V. These VCCs include CORVCC, DACVCC, IOVCC, MEMVCC AND DCKVCC. Therefore, all output signal levels are 3.3V or 5V with VOL rated at 0.5V and VOH rated at 0.7xVCC. All input and bi-directional I/O pads are designed to be 5.0V-tolerant, and the output signals may have external pull-up resistors to 5.0V.

When an output or I/O pad is actively driving a logic high level, the output level must not be forced above the graphics controller VCC level. A pull up resistor to +5V can be tolerated as long as the graphics controller IOL specification is satisfied when the pad is actively driving low. High-state IOH will then be limited by the 5V-to-3V drop across the pull-up resistor.

Stuffing options should be designed so that all VCCs are powered by 3.3V or 5V when the graphics controller is installed. If a DC/DC voltage converter is used to generate 3.3V or 5V, the output current rating must meet the graphics controller's power requirements as well as the requirements of other components which draw power from the same DC/DC voltage converter.

Panel Interface signals are 3.3V or 5V

All panel interface signals from the graphics controller are 3.3V or 5V (for those graphics controllers capable of operation at 5V), depending on the VCCs going in. Level-shifting buffer(s) should be added between the outputs of the graphics controller and the inputs of 5.0V panel if the graphics controller's VOL and VOH do not meet the requirements for panel's VIL and VIH. The signals involved include pins P0-P35, SHFCLK, LP, FLM, and M. Figure 1-1 shows a schematic of an example interface using IDT's 54/74FCT164245T. For 36-bit panels, pins P24-P35 can be buffered by an additional level shifter (U3) as shown in Figure 1-2.

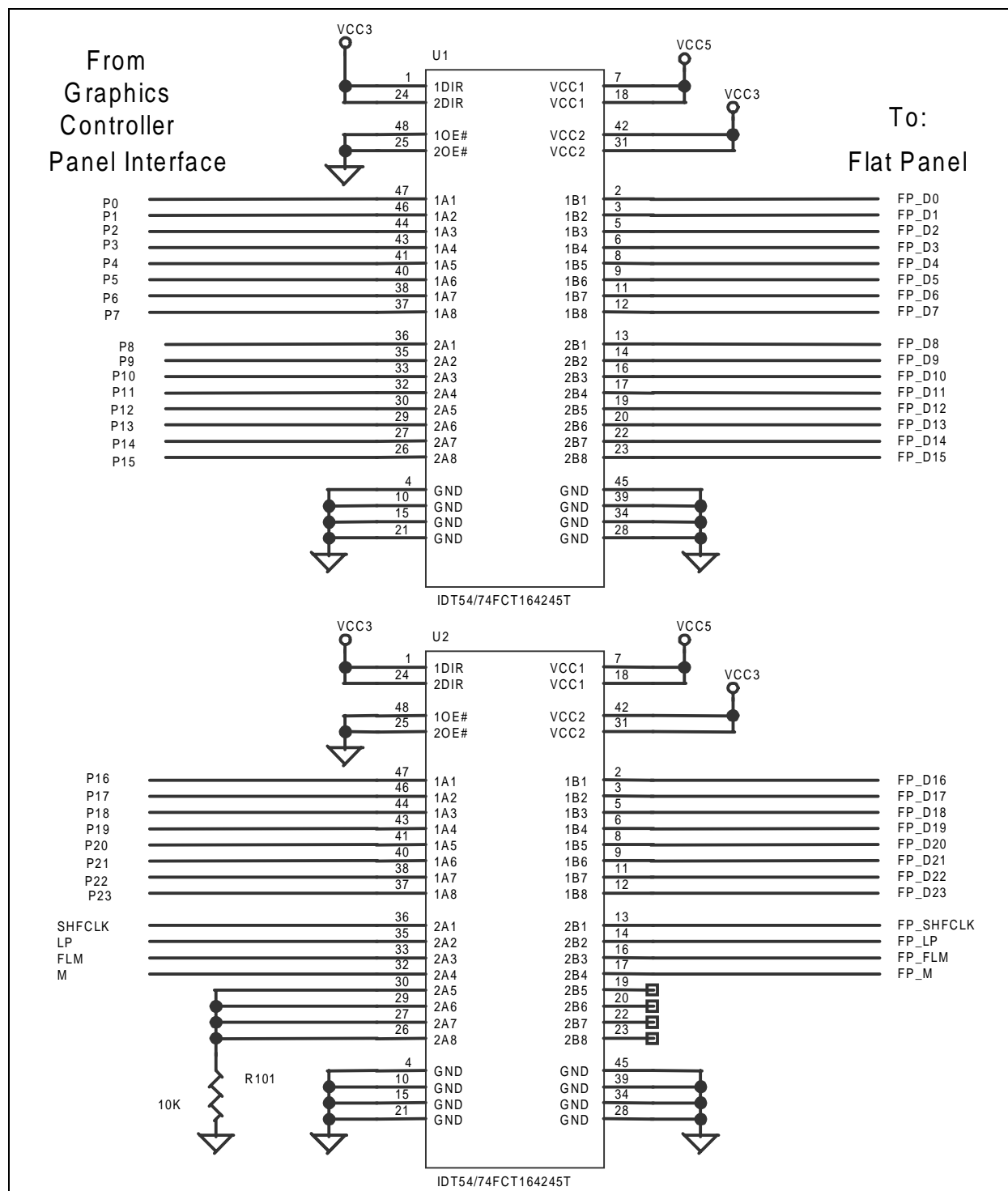


Figure 1-1: Interface connection using IDT's 54/74FCT164245T

CRT Hsync and Vsync are 3.3 V

To ensure full compatibility with older CRT displays, we recommend adding a 3.3V to 5.0V level-shifting buffer between the graphics controller Hsync and Vsync outputs and the display's Hsync and Vsync inputs whenever the VCCs are at 3.3V. Figure 1-2 shows a sample schematic of a level-shifting buffer (U3) which uses the IDT 54/74FCT164245T buffer.

Newer CRT displays that support DDC (Display Data Channel) clock and data signals are generally TTL compatible and should not require level shifting between the graphics controller and the CRT. The DDC signals are more difficult to buffer if they are not TTL compatible, because they are bi-directional. Additional control signals from the graphics controller would be needed to determine the direction of the level shifters. Fortunately, the graphics controller signals meet TTL compatibility requirements and do not need level shifters for TTL-compatible monitors.

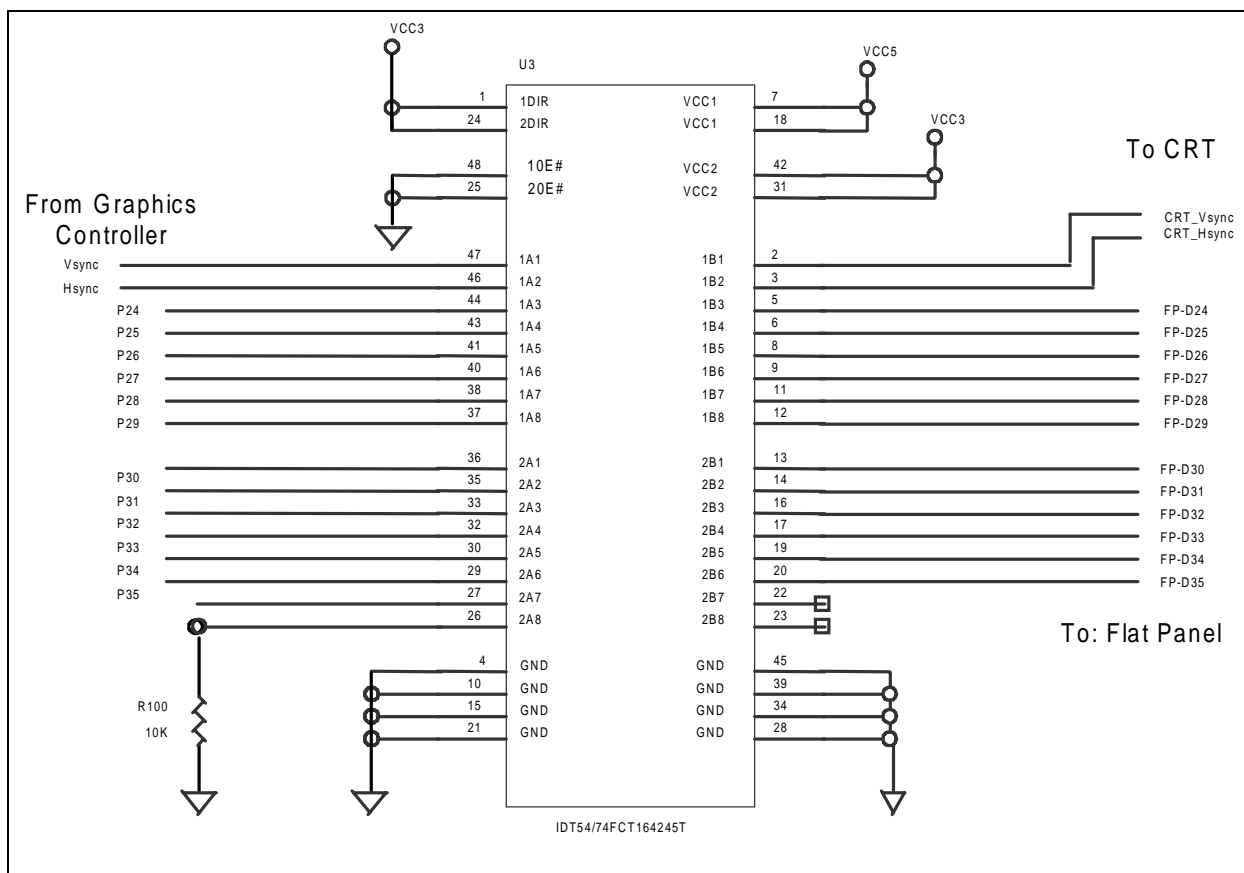


Figure 1-2: 3.3V to 5.0V Level-Shifting Buffer

5.0V/3.3V PCI Interface

The graphics controller does not require 3.3V to 5.0V level shifter buffers for PCI bus interface signals. The I/O pads for the graphics controller PCI signals are designed such that their AC and DC specifications meet the PCI requirements for both the 3.3V and 5.0V signal environments.

DRAM and EPROM

The 65550, 65554 and 65555 can operate with either 3.3V or 5V DRAM and EPROM. However, both the DRAM and the EPROM should be powered from the same voltage (that is, 3V for both or 5 V for both). This avoids any problems with a 3V DRAM or EPROM that is not 5V tolerant. This does not apply to the 69000.

HiQVideo™ Series - LVDS Interface for STN-DD or TFT Panels

Introduction

PCB designers may choose from a variety of options in graphics controllers, interface devices, and flat panel displays. However, optimal design performance and flexibility can be limited by FCC regulations regarding electromagnetic interference (EMI) and the needs associated with high bandwidth communication.

Speed, power, and EMI issues can be resolved by using CHIPS' HiQVideo™ graphics controller series coupled with the Low Voltage Differential Signaling (LVDS) technology available from National Semiconductor or Texas Instruments on STN-DD or TFT flat panels. Currently, our graphics controller provides the lowest clock jitter among VGA controllers in their class to work reliably with LVDS technology. Since Texas Instruments' Flatlink chipset, which consists of a transmitter (SN75LVDS81) and a receiver (SN75LVDS82) is compatible with National Semiconductors Flat Panel Display (FPD) Link chipset, the following paragraphs will only use FPD Link chipset as an example.

Product Overview

The purpose of LVDS is to reduce EMI and allow greater distances between the VGA controller and panel by sending only differential signals across the cable. Fewer active signals with a low-voltage signal swing reduce noise. Well-matched cable impedance minimizes signal reflections and standing waves.

One Flat Panel Display (FPD) Link chipset from National Semiconductor consists of a DS90C583 LVDS transmitter and a DS90C584 LVDS receiver connected by a cable containing four differential signal pairs for data and one differential signal pair for a 1X clock. See Figure 1-3 below. The transmitter receives 28 data bits (parallel) and a 1X transmit clock (20 to 65 MHz). The 1X clock is passed to the receiver over the clock differential pair. Both the Transmitter and Receiver contain their own phase-locked loops (PLL) which generate an internal 3.5X or 7X clock from the 1X clock source.

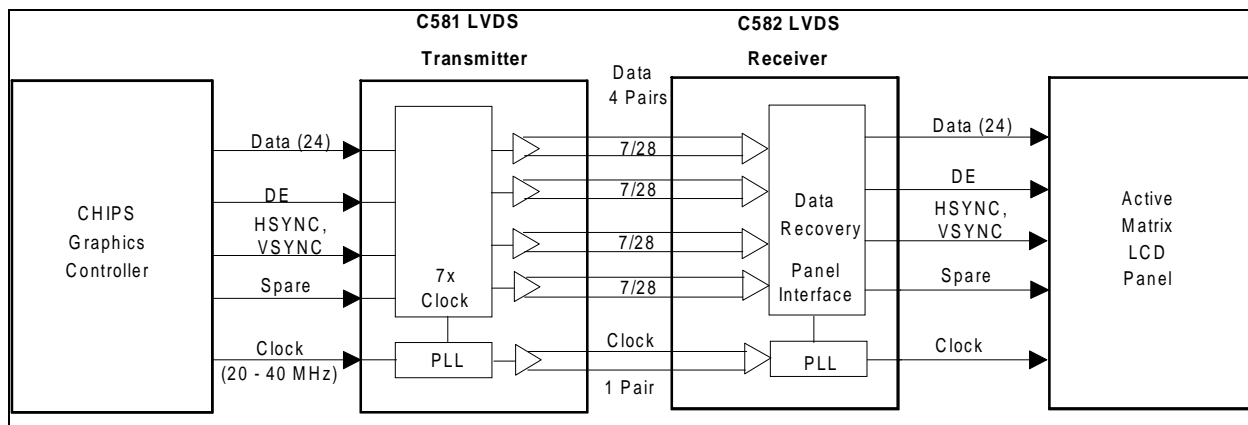


Figure 1-3: The DS90C583/584 LVDS Flat Panel Display (FPD) Link Chipset

The high frequency clock in the transmitter sends 7 of the 28 incoming data bits on each of the four differential data pairs during each cycle of the 1X clock. All 28 parallel data bits are transmitted over the four differential pairs during each 1X clock cycle. There is no encoding of the differential data bits. They are mapped directly from the incoming bits.

The high frequency clock in the receiver is used to convert the incoming differential data signals back into 28-bit parallel form. The 1X clock from the link is also passed on in single-ended form as an output from the Receiver. The Receiver relies on the 1X clock to define the field boundaries of the 7-bit serial streams on each differential data pair.

The 28 data bits are intended to consist of 24-bit pixel data plus DE, HSYNC, VSYNC, and one spare. There is no distinction between these functions within the LVDS link. All 28 bits are treated the same and passed over the link transparently. (For a 16-bit STN-DD panel, 16 of the data bits could be used for panel pixel

data (3 bpp RGB) and one of the 28 bits might be used for SHFCLK. The 11 remaining bits could be used for control signals such as DE, HSYNC, VSYNC, etc.)

The DS90CR583/4 synchronize the 28-bit parallel data to the rising edge of the 1X clock, while the DS90CF583/4 synchronize to the falling edge. Maximum throughput of the LVDS Link is 28 bits (3.5 bytes) per 1X clock. If the 1X clock is 65 MHz, the resulting throughput capability is $3.5 \times 65 = 227$ MB/sec. LVDS technology relies on phase-locked loops (PLL) to generate a much higher clocking frequency than the incoming pixel clock. This requires the incoming clock to be continuously running and very constant in frequency. The SHFCLK output from the graphics controller works well for the LVDS clock when interfacing to TFT panels. However, the SHFCLK generated for STN-DD panels does not meet LVDS PLL requirements because it may be stopped during blanking, may not be of a constant frequency, or may be too low in frequency.

VGA controllers generally use their own PLLs to generate the pixel clock. Depending on the quality of the PLL design, the quality of the external reference oscillator, and variable internal delays, there will always be some level of "jitter" in the resulting pixel clock available for LVDS use. Too much jitter can interfere with the ability of the LVDS PLLs to achieve a stable lock.

This applies to all LVDS applications, TFT as well as STN-DD.

24-Bit STN-DD Panels

Newer STN-DD panels may use a 24-bit panel data word instead of 16-bit, with eight pixels per word (3 bpp). For these panels, the ratio of pixels to panel clock cycles is an integer (8), so the SHFCLK frequency will not have missing pulses. However, it may still be necessary to force the panel clock low during blanking. There are two possible solutions:

- 1) Pass SHFCLK through as a data signal, and use a higher frequency DCLK for the LVDS clock, just as with 16-bit color STN-DD panels. A potential disadvantage of this approach is that the LVDS link may be limited to 28 signals. With 24 signals used for data and one for SHFCLK, there are only three signals available for controls such as VSYNC/FLM, HSYNC/LP, and DE. This may not be enough for some 24-bit panels.
- 2) A fourth control signal can be made available by using a free-running SHFCLK as the LVDS clock. This will add a gate on the panel side to force the panel clock low during blanking (DE low). This approach requires an external gate between the LVDS receiver and the panel, but allows up to four control signals to pass through a 28-bit LVDS link.

36-Bit TFT Panels

High-resolution TFT panels may use a 36-bit data word with two 18-bit pixels packed into each word (18 bpp color depth). This allows a lower pixel clock frequency (half-frequency) to be used, as compared to transferring only one 18-bit pixel per clock in an 18-bit panel data word.

One way to handle a 36-bit panel interface using 28-bit LVDS devices is to use two LVDS transmitter chips and two LVDS receiver chips to implement the equivalent of two separate 18-bit LVDS channels. One channel can be clocked on the rising edge of SHFCLK, while the other channel is clocked on the falling edge. The result is that one channel transfers the even numbered pixels and the other channel transfers the odd numbered pixels. The VGA controller provides one 18-bit pixel on each edge of SHFCLK, and the two LVDS receivers present a total of two pixels to the panel on each complete cycle of SHFCLK. This approach should work well with the graphics controller although it has not actually been tested by CHIPS.

In the graphics controller, the bit that enables one pixel on each edge of SHFCLK is FR12[0].

References

The summary of LVDS operations is based on the National Semiconductor DS90Cx581/582 Data Sheet and related Application Note, "An Introduction to FPD Link."

Self-Refresh DRAM in CRT-Only Mode

4/98

Note: This does not apply to the 69000.

In **CRT-only** mode, the 65550, 65554 and 65555 do not initiate the old-style self-refresh by sending a sequence of 512 CAS before RAS cycles.

Recommendation:

Use standard refresh modes, not self-refresh modes. When entering CRT only mode (FR01 bits 1 and 0 set to 01), always set FR05 bit 6 to 1. Setting this bit enables the non-self refresh function for DRAMs. This setting requires either an external 32KHz or an internal 37.5KHz clock (derived from 14.318MHz) to be used as the DRAM refresh clock in standby mode.

For customers that have neither an external 32KHz clock nor internal 37.5KHz reference clock (14.318MHz clock is stopped in standby mode), the following sequence provides for smooth transitions to and from standby mode.

- 1) Set FR05 bit 3 to 1: set to panel off mode
- 2) Set FR01 bits 1 and 0 to 10: enable flat panel mode
- 3) Go to Standby
- 4) Resume

Note: No action is required if the system is in panel-only or simultaneous mode before entering standby mode.

Chapter 2

PCB Layout Concerns

Guidelines for Using PBGAs in Surface Mount Technologies

Introduction

In general, the differences between the use of standard surface mount components such as Plastic Quad Flat Packs (PQFP), Thin Small Outline Package (TSOP), discrete components, and Plastic Ball Grid Arrays (PBGA) are very minor. This CHIP TIP discusses the pads and vias for the BGAs, the pad layout, reflow and rework of the chip.

Pads and Vias

Pads may be either Solder Mask Definable (SMD) or Non-Solder Mask Definable (NSMD). Tests have shown that there is no reliability implication of either method. The SMD method is more forgiving of rework while the NSMD method allows for somewhat denser routing. Unless there is a compelling reason to use NSMD pads, SMD pads are generally recommended.

Do not use vias in pads. The presence of the via depletes the solder in the balls and reduces the reliability and thermal properties of the package.

Layout

The typical configuration of the pads is a dog bone, with the exposed land at one end and a solder masked via at the other end. See Figure 2-1 below. The via should be about 0.3mm in diameter and its associated pad should be about 0.65mm in diameter. A typical SMD pad would have a 0.58mm open pad area with a 0.012mm overlap of solder mask over the copper.

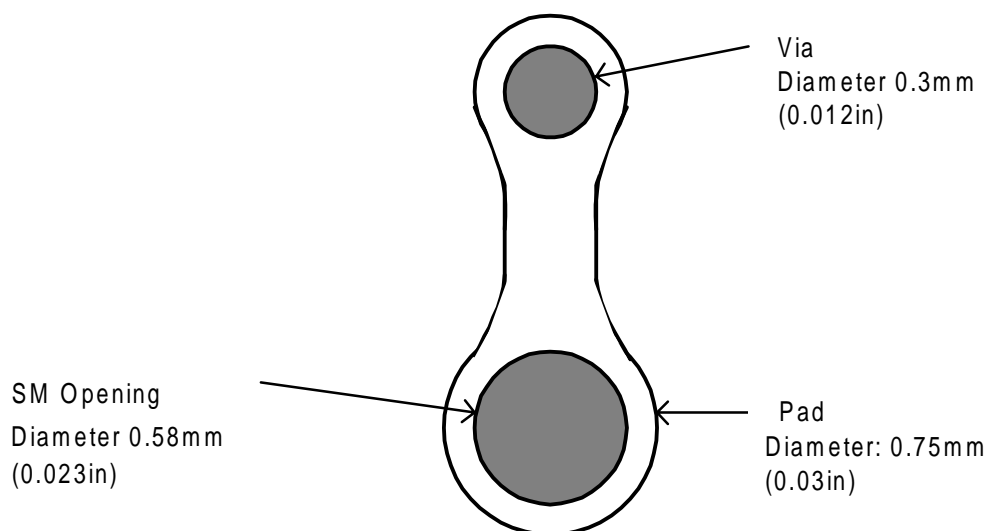


Figure 2-1: Dog Bone Solder Pad

Since there are no visual clues in the vertical direction to assist in the positioning of the chip, the user must either use a very low angle visual system or, more commonly, provide fiducial marks to align the package edge. The edges of the package are precisely defined and perfectly suitable for this purpose.

Because of the strong surface tension forces on the liquid solder surface during reflow, PBGAs tend to self-center themselves on the array of pads. Industry practice has shown that the packages misaligned by as much as 50% of a ball diameter can center themselves. Some users employ this property by creating oversized pads in the corners of their pad arrays to enhance self-centering.

Chips offers BGA packages which have 1.27mm ball spacing. To facilitate the routing of the motherboard, it is usually necessary to route connections to the inner two rows of balls to the depopulated area in the center of the package on the top metal and then out on another layer.

In the packages with a peripheral array of balls (such as all BGAs from CHIPS), there is a square array of balls in the center of the package. These balls are at the chip ground, and must be tied to ground. These balls also provide a conduit for drawing heat out of the package and into the ground plane of the motherboard. Prudent practice would be to leave the complete top copper foil with SMD pads under those balls and have multiple vias connecting to the motherboard ground plane. The connecting foil in the ground plane should be made as large as is practical to spread the heat over the largest possible area.

Reflow

Both water rinsable and no-clean fluxes work well with PBGAs. Remember that BGAs typically have much closer clearances than PQFPs so allowances must be made to assure thorough cleaning. The no-clean fluxes are becoming more popular in the industry.

Soldering can occur using paste screened on the lands or merely with the application of flux over the pads. The application of paste is somewhat critical because too much paste could result in ball-to-ball shorting. The recommended procedure uses the flux-only application because it does not have this problem. The most significant difference between the two procedures is that the BGA profile has a slightly lower maximum allowable temperature for the reflow cycle. While 230°C is the maximum allowable temperature, it is strongly recommended that the temperature be kept below 220°C unless the customer maintains stringent measures to keep the moisture level low in the packages. As an example, Figure 2-2 shows a typical reflow cycle. The individual user must, however, optimize the cycle to accommodate for the particular situation involved.

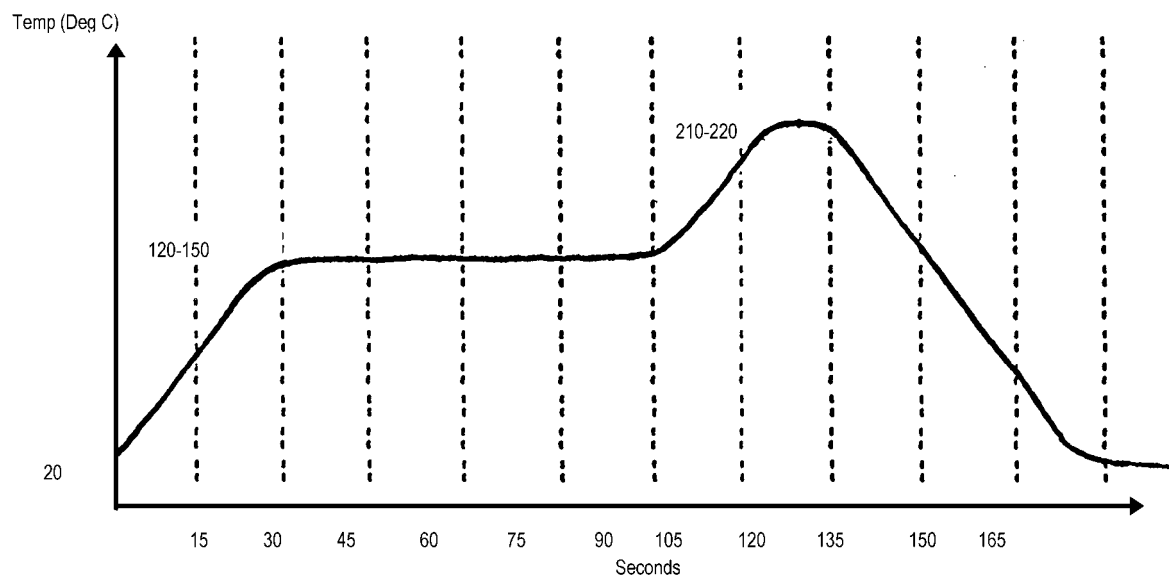


Figure 2-2: Typical I.R. Soldering Profile for BGAs

Rework

Because of the inability to inspect the solder joints on a BGA, users sometimes make a default decision that the failing component on a defective board is the BGA. The user is cautioned against this assumption. Typical failure rate on BGA solder joints on a well-engineered reflow process is about of 33PPM (0.003%) compared to 330PPM (0.033%) for PQFPs. The BGA should only be removed after eliminating all other sources of failure.

As a rule, it is not possible to re-use an individual chip after it has been removed from a board. This is very similar to the industry experience with fine lead QFPs.

Figure 2-3 shows a typical configuration for the nozzle for PBGA chip removal. Note that the air flow is directed to the surface of the device rather than to its underside as is common with removal tools for ceramic BGAs. The backside nozzles are recommended for PBGA, since the board designers can space the devices more closely on the boards with this type of removal.

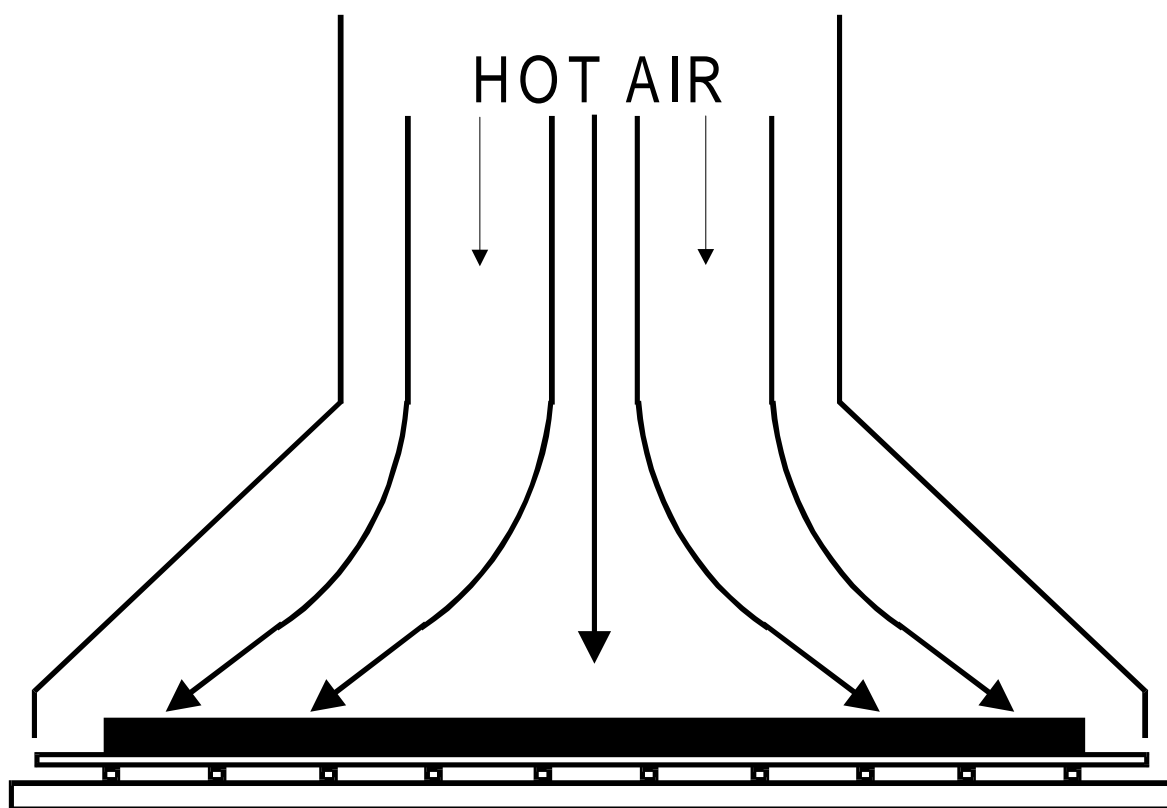


Figure 2-3: Typical Nozzle Configuration for PBGA Chip Removal.

After removing the chip, the residual solder remaining on the pads on the board should be removed with a suction device. All remaining solder should be leveled with hot air. The area for the replacement chip should then be fluxed, and the replacement chip applied.

Chapter 3

Video I/O

System Level NTSC/PAL Out Implementation

Introduction

The television display format is an old but complex standard and has not changed for the last few decades. In contrast, computer monitors have evolved from a monochrome, interlaced display into very advanced color and high resolution non-interlaced displays. There are fundamental differences that must be resolved when displaying a graphics image onto a television display. The graphics controller has built-in NTSC/PAL out flicker reduction circuitry to further enhance the television output display quality. To display a computer generated image on television, system designers must understand some of the differences between computer monitor display and television display.

System Design Considerations in Encoder selection

CHIPS selected the AD722/724 television encoder from Analog Devices as the reference design for the DK board. However, the graphics controller is not limited to this device. System designers may select from the many television encoders that vary in price and features.

The graphics controller provides a CSYNC signal by combining both the HSYNC and VSYNC (XNOR) and the analog RGB signals going to the AD722/724. A reference clock of either 14.318180MHz for NTSC format or 17.734480MHz for PAL output is provided. The CHIPS design uses an external oscillator for the clock reference. One design option uses one quarter of the above frequencies and allows the internal PLL of the AD722/724 to generate the clock. CHIPS does not recommend this option because this clock must be very accurate. The AD722/724 processes these signals based on the input reference clock and then outputs three television signals: composite output, luminance output and chrominance output.

AD722/724 is a 5-volt part that requires V_{IH} at 4.0 volt. The graphics controller is a 3-volt process which outputs TTL level signals. In this case, the CSYNC signal requires a level shifter or some type buffer before entering AD722/724. Please consult the AD722/724 datasheet for further layout and design considerations.

Television Formats: Interlaced vs. Non-interlaced

Television is an interlaced display. Computer graphics have evolved into non-interlaced displays. Displaying an image that was generated for a non-interlaced monitor on an interlaced monitor causes flicker and other artifacts on the display. Interlaced monitors display even and odd fields alternately. Non-interlaced monitors display both fields simultaneously. Consider drawing a one pixel-wide horizontal line across the screen. The television will display this line only at either even or odd fields. Therefore, this line is displayed on every other field. Our eyes perceive this as flicker. Regular television programs are intentionally optimized for the television display and so reduce flicker.

SVIDEO

The AD722/724 converts RGB signals to YUV format, then generates luminance and chrominance output for the SVIDEO-in connector on television. Not every television has an SVIDEO-in input, however. CHIPS strongly recommends using SVIDEO-in when possible because the display quality is always better.

CSYNCH

The AD722/724 also combines luminance and chrominance signals to send out a composite output. This is the standard connector for all televisions. However, television must separate the luminance and chrominance signals by itself, and the recovered signals usually are not as good as the originals. Some of the higher-end televisions have built in comb filters which are good at improving the recovered display quality.

Accurate frequency

Television requires very accurate timing. For studio quality video, the subcarrier frequency must be within 10Hz. Unlike broadcasters who produce television shows, we do not want to fine tune each system in the production line to be within the 10Hz specification. CHIPS recommends using a 20ppm accuracy oscillator when providing the reference clock to the AD722/724. CHIPS also recommends using the 14.318180MHz or 17.734480MHz 4x clock instead of 1x clock because the frequency error increase when the internal PLL of the AD722/724 tries to increase the input frequency by 4 times. This experiment shows that most televisions can handle a +/-500Hz before television starts to turn off its color burst.

Flicker Reduction Using Vertical Averaging

Averaging two adjacent lines can reduce television flicker. This minimizes the difference between two lines which caused the most flicker. Using the same example from above, the horizontal line we draw will be averaged with next line. If the first line is black and second line is white, the first will display the average of two lines, which is gray. The second line will display a color depending on the third line. For our purpose, we make the third line white to make this case simple. In this example, the second line will display white. As shown, alternating gray and white between two fields is not as disturbing to human eyes as alternating black and white. This is why vertical averaging significantly reduces flickers on television. Performing additional line averaging could further reduce television flicker, but it also significantly reduces the readability of the static images, motion video, and text. When too many lines are averaged, text becomes too blurry to read because the pixels collapse. The graphics controller performs two line averaging, since this is a good balance between flickering and text readability (the graphics controller also performs three pixels horizontal averaging for further flicker reduction).

Overscan

Television broadcast resolution is always higher than what a normal television can display. To work around this, television broadcasting studios leave additional blank spaces around the image so viewers see the whole image. Computer generated information uses the whole screen including those extra blank spaces. This creates a problem. Viewers will see only partial image because some of the information remains outside of the television display area. For NTSC, the overscan resolution is 480 lines. A normal television displays about 384 lines. Some televisions can display over 400 lines.

To address this issue, the graphics controller will perform panning in DOS modes. The graphics controller will either pan or select a lower resolution in the Windows environment. For example, NTSC should display 480 lines. Since most televisions display only 400 lines, we can select 640 x 400 resolution in Windows in order to see the whole screen. Horizontal overscan is not a problem because we are able to fit the whole image in by increasing the dot clock.

Artifacts

There are some artifacts on television display. Some can be eliminated, but some can only be minimized. We need to understand the cause before we can optimize television out display quality.

Shadows

When displaying an icon, we sometimes see shadows behind the icon. The most likely is the inaccurate horizontal sync frequency. Adjusting the horizontal frequency so that it is 15.734KHz for NTSC and 15.625KHz for PAL can minimize the shadow.

Dot Crawl

Dot crawl is a type of distortion that shows up on the boundary of two different colors. It looks like a moving dot pattern continuously scrolling in one direction. It can move upward, downward or diagonally. Television is inefficient in differentiating between luminance and chrominance data. Therefore, the dot crawl will always be there. However, by adjusting the CRTC parameters, the graphics controller can control the dot crawl so that it is less noticeable. We can make it move slow, fast or not at all. The only way to completely remove dot crawl is to use the SVIDEO input.

Waving

Waving is another concern. It is mostly caused by CSYNC timing imperfectly matched with the reference clock that goes to AD722/724. This reference clock should keep in a phase relationship to the reference clock that goes to the graphics controller in order to minimize waving. When our Dot clock is running asynchronously to AD722/724, the display may not look good due to waving. If system designers can use the same clock for both reference clocks, this artifact is usually reduced.

Color Text

When luminance data is switching at a frequency that is too close to color burst frequency, television may misinterpret as it color information and display it as color. This is most common when displaying text, because text is usually has a black background and a white foreground, or vice versa. They are usually two pixels wide, so the toggle rate is at a frequency that is very close to color burst frequency. This result displays text, but that text will be in a different color. Since the AD722/724 does not have a Y trap filter built in to solve this type of problem, the best solution is to fine tune the CRTC parameters and dot clock so the timing is farther from the color burst frequency. However, the waving will return if the frequencies are too far apart.

Summary

Chips and Technologies, Inc. provides utilities such as DEBUGVGA, MODETEST, and a NTSC/PAL Out mode switching program in Windows which allows designers to fine tune their NTSC/PAL Out display quality. Without some of the commands in DEBUGVGA, fine tuning the CRTC parameters could be very difficult. Our BIOS has been tuned for the best display quality. Because display quality is very subjective, system designers may want to make additional adjustments. We selected the AD722/724 for a reference design because it is the simplest television encoder. It does not change our signal timing for NTSC/PAL Out. Instead, it takes our output signals, encodes them into composite synch, and sends it to the television. It is the most straightforward device, which we feel translates into low design cost.

Implementing DVD with External MPEG2 Decoders

DVD offers the promise of incredibly huge storage capacities (up to 17 GB) for information and software, richly entertaining 3-D games, and above all, theater-quality movies playable on either stand-alone DVD home entertainment players or on the flat panels and CRT displays of personal computers.

The widespread market acceptance of existing CD-ROM technology has already thoroughly validated the viability of such a medium for personal computers and high-quality consumer audio. With the greatly expanded storage capacity of DVD, combined with highly efficient compression technologies such as MPEG2, the technology has reached the threshold at which it becomes feasible to store an entire two-hour theater-quality movie on a single DVD disc, for playback on either a personal computer or a stand-alone home entertainment player.

8-Bit and 16-Bit YUV Interfaces

The interfacing concept is very simple, as shown in Figure 3-1. Leading-edge DVD solutions from vendors such as C-Cube, Zoran (SGS-Thompson) and IBM already provide a direct interface to off-the-shelf TV encoders such as the Philips SAA7182, Brooktree Bt856, and Analog Devices ADV7176A. These interfaces between the MPEG2 decoder chip and the TV encoder typically utilize 8-bit or 16-bit digital YUV 4:2:2 format, compliant with CCIR-601-2 and/or CCIR-656 standards. That same interface is directly compatible with the video data port of the graphics controller, with only minor TTL "glue" logic potentially needed for 8-bit to 16-bit data conversion.

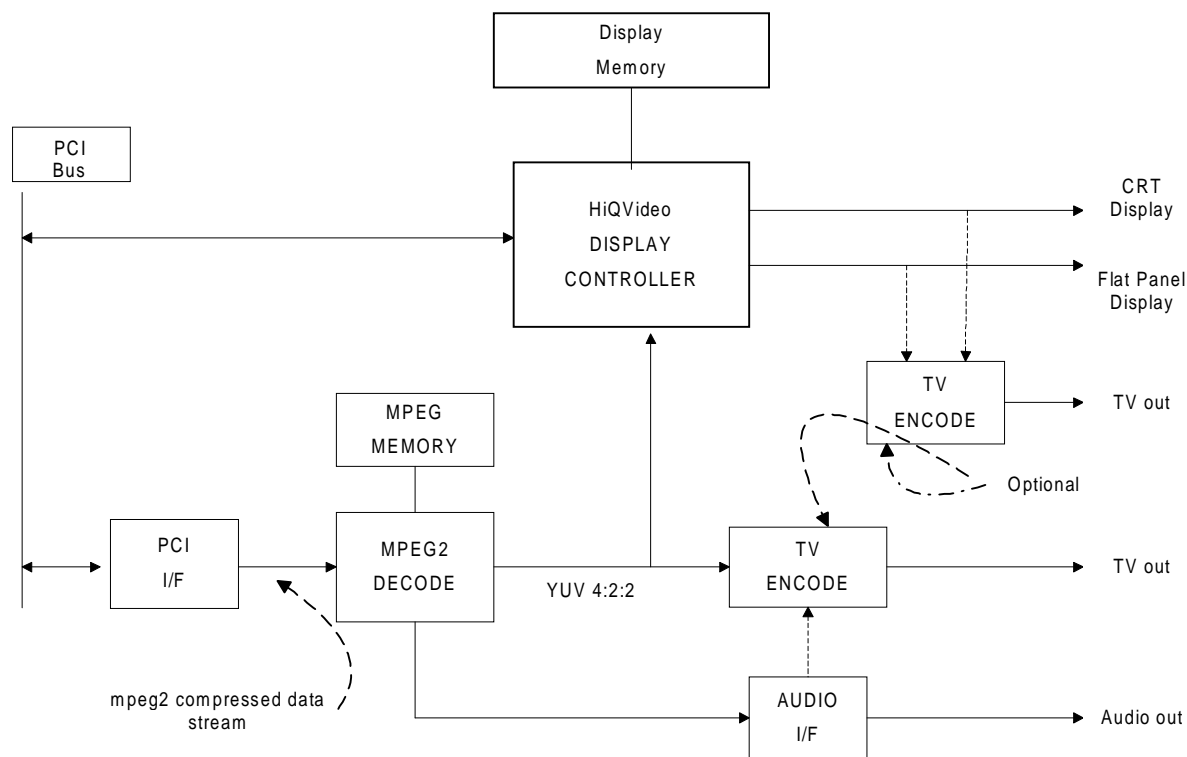


Figure 3-1: General DVD Block Diagram

The video data port of the graphics controller is designed specifically for compatibility with the Philips SAA7110 and PCMCIA ZV-Port specifications and supports 16-bit YUV 4:2:2 (CCIR-601-2). A simple TTL "glue" circuit, described in more detail below, can assemble 8-bit YUV 4:2:2 into the 16-bit form needed by the graphics controller.

The graphics controller does not support newer aspects of CCIR-656 such as the SAV and EAV coding patterns (Start and End of Active Video) in the data stream in lieu of separate HREF and VREF synchronization signals. This is not a problem, however, because most leading-edge DVD solutions support the original CCIR-601-2 standard with or without the newer CCIR-656 features.

Typical DVD Reference Designs

DVD reference designs are currently available from a number of vendors, including C-Cube, Zoran and IBM. Figure 3-1 shows a general block diagram applicable to all of these designs. In many cases, the technical documentation for these reference designs is currently available only under non-disclosure agreements. These vendors should be contacted directly for full details.

The main hardware elements used in some or all of these reference designs are as follows:

- MPEG2 decoder chip, such as the C-Cube ZIVA-D6, the SGS-Thompson STi3520A or the IBM MPEGCD1M.
Note: DVD anti-copy protection (decryption) may require an external IC if not integrated into the main MPEG2 device.
- TV encoder chip, such as the Brooktree Bt856, the Philips SAA7182 or Analog Devices ADV7176A.
Note: TV encoders that implement Macrovision anti-copying protection are needed for production designs to comply with DVD licensing requirements, and for DVD software compatibility for displaying encrypted DVD content. The TV encoder may be connected to the output of the graphics controller rather than that of the MPEG2 decoder, to allow TV display of computer graphics as well as MPEG2 content. However, DVD licensing requirements should be reviewed carefully before deciding exactly where to place the TV encoder and what type of encoder to use.
- PCI interface and control logic to provide the main pathway for the compressed MPEG2 data stream and to allow host software to control the overall decode process.
Note: Devices such as the Zoran ZR36120 or the AMCC S5933 may be used. IBM's MPEGCD1M goes one step further, integrating the interface and control logic with an MPEG2 decoder. There may well be a need for further control logic provided by a programmable logic device.
- Audio decoding with a speaker output of 2 or 6 channels provided by such parts as a Zoran ZR38520 or ZR38521 DSP, Motorola's DSP56011 decoder, a Burr-Brown PCM 1721 or PCM 1717E DAC, or a Crystal CS4331 DAC.
- MPEG buffer for the decoding process, typically at least 2 or 3 MB in size.
- Clock generators for MPEG pixel timing and horizontal/vertical sync. The frequency requirements are discussed further below.

Some of the reference designs also include additional IC's that are not necessary with the graphics controller:

- YUV-to-RGB conversion in hardware and transfer of decoded MPEG data across the PCI Bus directly into the graphics display memory to support graphics controllers that do not possess the video data port of the graphics controller. Use of the video data port for a direct connection to the output of the MPEG2 decoder dramatically decreases the PCI bus traffic. The use of a YUV-compatible video data port on the VGA controller normally provides a more effective overall system solution for DVD playback.
- Video scaling and color-keyed overlay on a CRT display by intercepting the analog RGB output from the VGA controller. Again, the use of the video data port of the graphics controller provides a better alternative, making costly external IC's unnecessary in implementing these functions.

TV Encoder

A TV encoder is not needed in PC designs that are intended to support DVD playback on CRT and/or flat panel displays only. However, in designs that do need to be able to drive a television receiver, there are three potential options for the placement of the TV encoder, as indicated in Figure 3-1:

- Drive the TV encoder directly from the MPEG2 decoder. This approach does not allow computer graphics information to be displayed on the TV screen, but it does allow the CRT and/or flat panel displays to remain active at the same time that the TV interface is active, unlike the other two solutions, below.
- Drive the TV encoder from the analog RGB outputs provided by the VGA controller device. Unfortunately, there is a DVD licensing requirement for Macrovision anti-copying protection in systems that can play encrypted DVD content such as Hollywood movies, to discourage casual copying. No TV encoder has so far been identified that provides the Macrovision algorithm and also accepts analog RGB as an input. All known Macrovision-equipped encoders require some form of digital input, most commonly 8-bit YUV.
- Drive the TV encoder from the digital RGB flat panel outputs provided by the VGA controller device. Unfortunately, the only available TV encoder identified to date that supports both 24-bit digital RGB input and Macrovision anti-copy protection is the Brooktree Bt857, but even that solution does not meet the latest DVD and PC98 requirement for Macrovision Version 7 or higher. Furthermore, because of the timing differences between TV receivers and computer displays, both this approach and the analog RGB approach require the CRT and panel interfaces to remain disabled when the TV output is active. The additional circuitry to disable the CRT or panel interface when using TV output is not represented in Figure 3-1.

TV encoder manufacturers should be contacted directly for advance information on unannounced future products designed to support Macrovision Version 7.

Pixel Clocking Requirements

In YUV 4:2:2 sampling, pixels are grouped into pairs. The first pixel of each pair has both a luminance or intensity value (Y) and a chrominance or color value (Cb, Cr). The second pixel of each pair has a luminance (Y) value only. Refer to Appendix A and CCIR-601-2 for further explanation of how Y, Cb and Cr relate to R, G and B.

"Pixels" technically exist only after the original video image has undergone a "sampling" process. CCIR-601-2 specifies a fixed (orthogonal) sampling rate of 13.5 MHz for both NTSC and PAL television systems. The horizontal and vertical sweep rates are derived from this 13.5 MHz master frequency using integer divisors, with different divisors for PAL as compared to NTSC.

Since MPEG2 decoders typically generate 8-bit YUV 4:2:2 output, the usual pixel clock frequency requirement for MPEG2 decoders is 27 MHz, exactly double the CCIR-601-2 pixel sampling rate of 13.5 MHz.

The clocking order for 8-bit and 16-bit versions of YUV 4:2:2 is as follows:

8-bit: Cb0, Y0, Cr0, Y1, Cb2, Y2, Cr2, Y3, Cb4, Y4, Cr4, Y5, Cb6, ...
16-bit: Cb0:Y0, Cr0:Y1, Cb2:Y2, Cr2:Y3, Cb4:Y4, Cr4:Y5, Cb6:Y6, ...

"Cb0:Y0" means 8 bits of chrominance (Cb0) and 8 bits of luminance (Y) in the same 16-bit word.

Since the average number of bits per pixel is 16, and since the graphics controller utilizes 16-bit YUV, the VCLK frequency needed by the graphics controller is the same as the pixel rate, namely, 13.5 MHz (not 27 MHz).

Pixel Clock Generator & Y-Latch

The 13.5 MHz VCLK frequency can be generated by dividing the 27 MHz MPEG2 clock by 2 with a JK flip-flop as shown in Figure 3-2. HSYNC# is used to synchronize the 13.5 MHz clock to the proper byte (Y or Cb/Cr) in each byte-pair. A simple octal register captures the luminance byte (Y) for each byte-pair, while the chrominance byte drives the graphics controller video data port directly. The luminance bytes are always latched halfway into the 13.5 MHz video clock cycle.

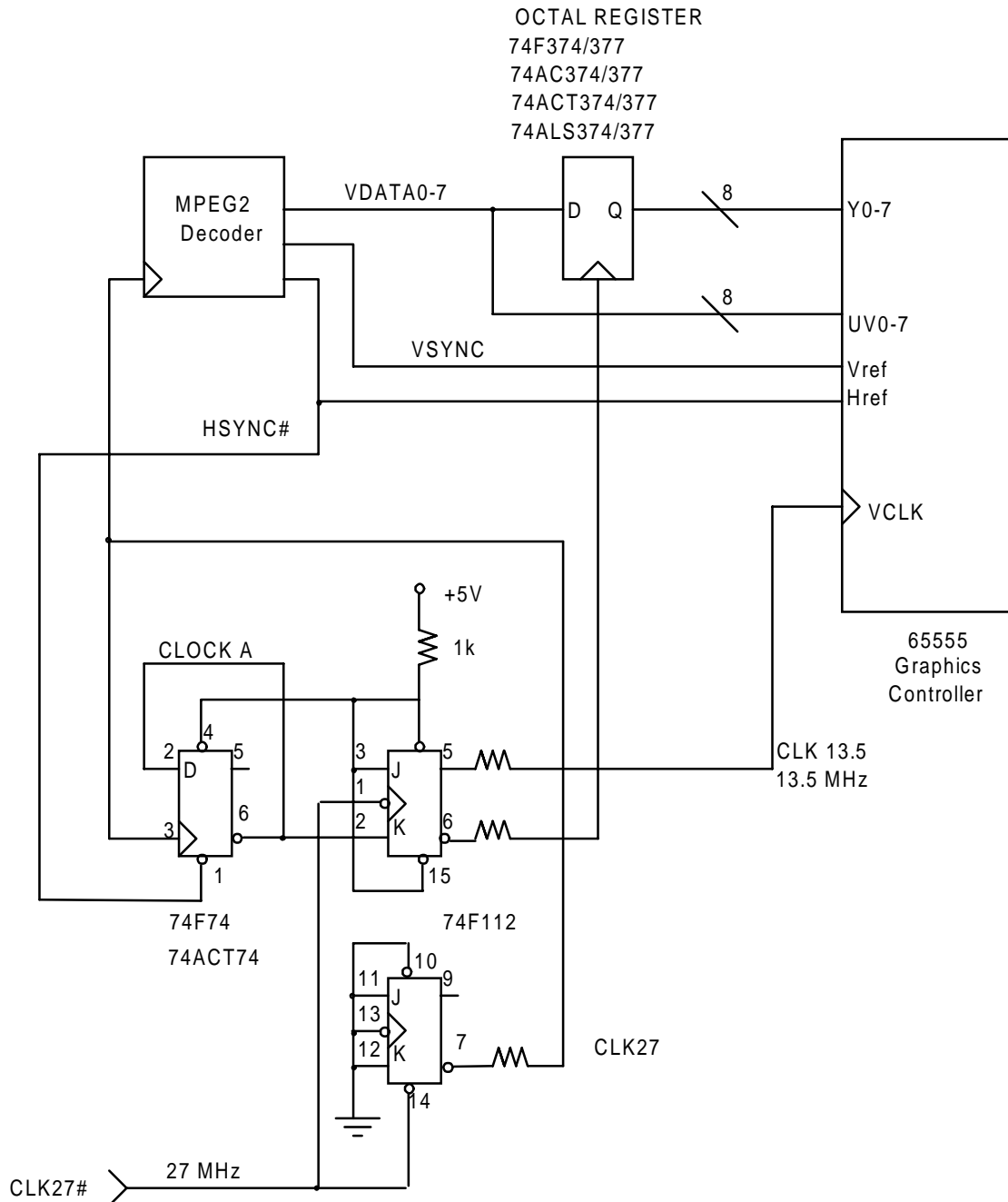


Figure 3-2: 16-bit YUV 4:2:2 Interface

A second JK flip-flop (CLK27 output) acts as a simple inverter having very nearly the same propagation delay as the CLK13.5 flip-flop. This results in very low skew between CLK27 and CLK13.5. Due to the short hold time (3ns worst-case minimum) at the MPEG2 decoder output, low skew is extremely important to prevent hold-time violations at the Y-latch and/or the video data port of the graphics controller.

Various factors arising from the use of a 74F112 IC ensure low skew from the JK flip-flops depicted in Figure

3-2. Use of a 74F112 IC allows both flip-flops to be within the same package, thereby maintaining nearly identical environmental conditions (temperature and VCC) and process characteristics. The 74F112 flip-flops have inherently low clock-to-output propagation delays -- 7.5 ns worst-case maximum, which is better than other devices such as the 74F74 or 74ACT-series devices. The specified 74F112 propagation delay for CD-to-Q# is the same as for CP to Q or Q#, namely, 2 ns minimum to 7.5 ns maximum. As a result, the overall delay from 27 MHz input to 27 MHz output (inverted) matches the delay from 27 MHz input to 13.5 MHz output very closely.

Figure 3-3 shows the synchronizing effect of HSYNC#. When HSYNC# is low, clock A is held high. This allows CLK13.5 to toggle on every CLK27 cycle, producing a 13.5 MHz output. The rising edge of HSYNC# allows clock A to begin toggling. Whenever clock A is low, CLK13.5 is forced high on the next CLK27 cycle. If CLK13.5 was already high, it simply stays high for two consecutive CLK27 cycles as shown in Figure 3-3. The result is that CLK13.5 and clock A toggle in phase.

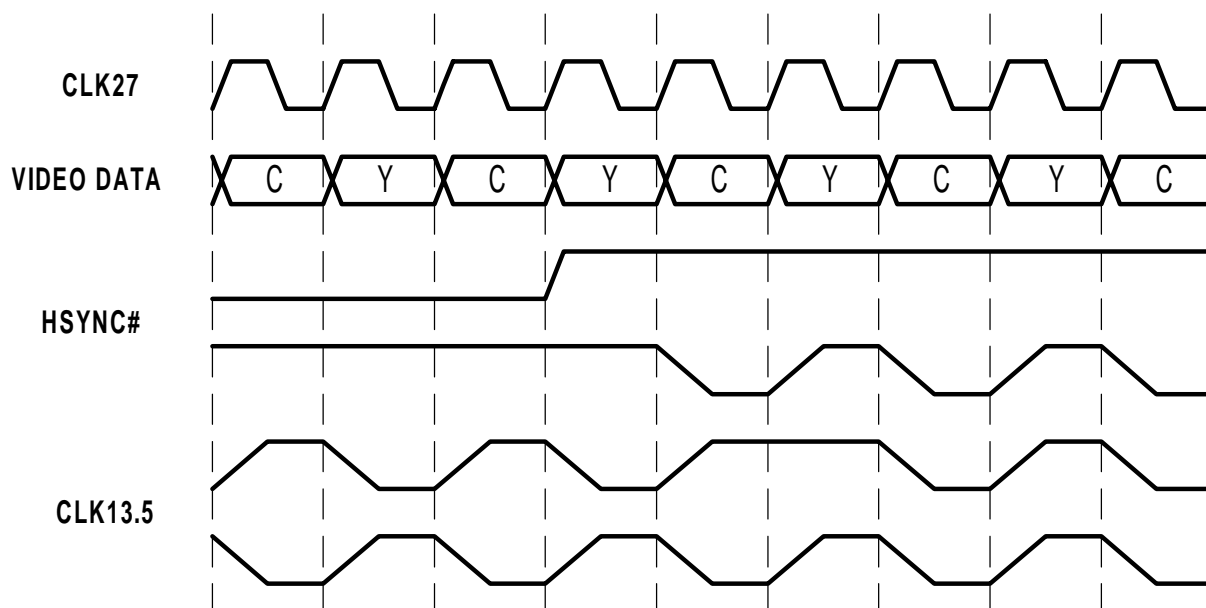


Figure 3-3: 13.5MHz Clock Timing

It should be noted that this design can cause a short pulse to occur on clock A on the falling edge of HSYNC#, but such a pulse from the 74F74 will not disturb the JK flip-flop because the pulse will have ended before the next CLK27 cycle begins.

The phase synchronization of CLK13.5 assumes that the rising edge of HSYNC# coincides with the start of a "Y" cycle of CLK27. If the MPEG2 device chosen for the design provides the opposite relationship, i.e., HSYNC# rise during a Cb or Cr cycle, then the J and K inputs on the CLK13.5 flip-flop should be reversed. Tie the J input to clock A, and tie the K input to a pull-high resistor. Once clock A and CLK13.5 have become synchronized to the proper phase of CLK27, there should never again be a loss of phase.

Since CLK13.5 continues running while HSYNC# is low (with at most one elongated cycle when HSYNC# returns high), the polarity of HSYNC# doesn't matter. The CLK13.5 synchronization mechanism can operate with either a "mostly high" HSYNC# or a "mostly low" HSYNC#. In addition, the HSYNC# polarity expected at the video data port is programmable (MR02 bit 4).

Depending on worst-case MPEG2 decoder output delay for HSYNC#, the setup time for the 74F74 flip-flop may be as short as 7 ns. This is within the specification for either a 74F74 or a 74ACT74, but may not be within the capabilities of other flip-flop technologies. (The setup time for the CD input is more commonly

referred to as "recovery time" before CP rise.) For video data, the MPEG2 decoder output delay generally is 20 ns maximum or less, leaving 17 ns setup time for the octal latch and the data inputs of the video data port.

The three series resistors on the outputs of the JK flip-flops provide impedance matching to minimize ringing and reflections. The optimum resistor value will depend on circuit board layout, probably in the range of 20 to 33 ohms. Obviously, the resistors should be placed close to the 74F112 to minimize the trace lengths between the 74F112 and the resistors.

Test Results

So far, the C-Cube and Zoran reference designs have been tested successfully in our lab, using the 16-bit YUV interfaces already present in those designs. The IBM reference design will be tested as soon as practicable, subject to availability of hardware and software. We have not yet tested the clock generator and latch depicted earlier in Figure 3-2, but it follows the basic design concept found in all of the reference designs.

A Brief Explanation of YUV, NTSC & PAL

As specified in more detail in CCIR-601-2, the relationship between YCbCr (also known as YUV) and the original RGB source information (after gamma pre-correction) is as follows:

$$Y = 0.299 \times R + 0.587 \times G + 0.114 \times B$$

Y, R, G, and B are all analog values varying from 0 to 1. Y represents the overall intensity or luminance of the sample. The chrominance components are defined as follows:

$$Cb = B - Y, \text{ normalized so that } Cb \text{ varies from } -0.5 \text{ to } +0.5.$$

$$Cr = R - Y, \text{ normalized so that } Cr \text{ varies from } -0.5 \text{ to } +0.5.$$

$$\text{Thus, } Cb = (B - Y) / 1.772 = -0.169 \times R - 0.331 \times G + 0.500 \times B$$

$$Cr = (R - Y) / 1.402 = 0.500 \times R - 0.419 \times G - 0.081 \times B$$

"1.772" is the result of $(1 - 0.114) / 0.5$. "1.402" is the result of $(1 - 0.299) / 0.5$.

"Gamma pre-correction" refers to an adjustment of the original RGB to allow for the expected "gamma" or non-linearity factor of the television receiver. Refer to CCIR-601-2 for further details.

Note: If $R=G=B$ (as they do when the color is white, gray or black), then $Y=R=G=B$ and $Cb=Cr=0$. In other words, monochrome signals have luminance (Y) but no chrominance.

The overall purpose and result of YUV-based signal processing is to achieve a remarkably high degree of compatibility between monochrome and color TV signals and receivers. Color signals can be transmitted within the same bandwidth allowances originally established for monochrome broadcasting; color signals sent to monochrome receivers display as esthetically optimal shades of gray, similar to a black-and-white photograph of a color scene; and monochrome signals sent to color receivers look the same as on monochrome receivers.

The 8-bit digital representations for the RGB and YUV parameters are specified to have the following ranges:

For R, G, B & Y: 0 corresponds to 16, 1 corresponds to 235 (decimal).

For Cb, Cr: 0 ± 0.5 corresponds to 128 ± 112 (decimal).

Note: There are a number of unused 8-bit codes available for special purposes, as described in CCIR-601-2 and CCIR-656.

Timing Standards

CCIR-601-2 specifies two main timing standards for "4:2:2" sampling:

525-line, 60 field/sec (e.g., NTSC)

13.5 MHz sampling rate for luminance.

858 samples per total line, hence 15.734 kHz horizontal frequency.

720 active luminance samples per horizontal line.

16 luminance clocks from end of active line to start of HSYNC.

Interlacing, 2 fields per frame, hence, 59.94 Hz field rate.

625-line, 50 field/sec (e.g., PAL)

13.5 MHz sampling rate for luminance, same as with NTSC.

864 samples per total line, hence 15.625 kHz horizontal frequency.

720 active luminance samples per horizontal line.

12 luminance clocks from end of active line to start of HSYNC.

Interlacing, 2 fields per frame, hence, 50 Hz field rate.

CCIR-601-2 doesn't specify the number of active lines in a complete frame, but MPEG2 decoders generally provide output resolutions of 720 x 480 for NTSC (29.97 frames/sec), or 720 x 576 for PAL (25 frames/sec). Other MPEG resolutions generally are also supported as subsets of these. The corresponding blanking ratios are $(858 \times 525) / (720 \times 480) = 1.3$ for NTSC, or $(864 \times 625) / (720 \times 576) = 1.3$ for PAL. In other words, blanking and retrace add about 30% to the total frame time needed for active video.

REFERENCES

1. C-Cube Microsystems ZiVA-Card© Reference Design Kit, Version 1.1, June 20, 1997. (Confidential Document -- NDA required)
2. C-Cube ZiVA-D6 and ZiVA-DS Decoder User's Manual, 1997.
3. Zoran DVD4PC Technical Reference Manual, Version 1.2, September 1996. (ZORAN Proprietary Information)
4. SGS-Thompson STi3520A and STi3400 data sheets, 2/97 and 1/96, respectively.
5. IBM Functional Specification for the MPEGCD1M Test Card, March 1997.
6. CCIR-601-2 and CCIR-656 specifications, as reprinted in the 1994 Philips Desktop Video Data Handbook.
7. Application note, "Color space, digital coding, and sampling schemes for video signals," reprinted in the 1994 Philips Desktop Video Data Handbook.
8. "DVD '97 Tools & Strategies for the Multimedia Revolution," a White Paper by Nikkei BP BizTech, June 10, 1997.
9. "MPEG-2 Fundamentals for Broadcast and Post-Production Engineers," a White Paper from Tektronix, Inc., July 1996.

Chapter 4

Interfacing with Flat Panels

Interfacing to the Optrex DMF-50714NCU-FW 1024x768 DSTN 16-bit Interface, 4-bit packed, 5.0V

Panel General Description:

Resolution: 1024 x 768
Type: DSTN
Pixel Depth: 4 bit/packed

Display Color:
Display Area:
Pixel/SHFCLK:

Connection Tables with 55x Panel Connector CN1

Optrex Pin Name	Optrex Pin Number	Chip's Pin Number	Chip's Pin Name
FLM	1	11	FLM
VSS	2	6	GND
DISP_OFF	3	Connect to toggle switch, one side VCC and other side GND	-
CL1	4	10	LP
VSS	5	9	GND
CL2	6	13	SHFCLK
VSS	7	12	GND
UD0	8	31	UG2 (P11)
UD1	9	30	UR2 (P10)
UD2	10	28	UB1 (P9)
UD3	11	27	UG1 (P8)
UD4	12	19	UR1 (P3)
UD5	13	18	UB0 (P2)
UD6	14	16	UG0 (P1)
UD7	15	15	UR0 (P0)

Connection Tables with 55x Panel Connector (continued)

CN2

Optrex Pin Name	Optrex Pin Number	Chip's Pin Number	Chip's Pin Name
LD0	1	37	LG2 (P15)
LD1	2	36	LR2 (P14)
LD2	3	34	LB1 (P13)
LD3	4	33	LG1 (P12)
LD4	5	25	LR1 (P7)
LD5	6	24	LB0 (P6)
LD6	7	22	LG0 (P5)
LD7	8	21	LR0 (P4)
VDD	9	1	VDDSAFE
VDD	10	1	VDDSAFE
VSS	11	14	GND
VR	12	3	VEESAFE (typ +32V)
?? VEE/NC	13	NC	
?? VEE/NC	14	NC	

CN3

Optrex Pin Name	Optrex Pin Number	Chip's Pin Number	Chip's Pin Name
VR1	1	Pin 1 of 10K Ω resistor pot (see Note 1)	-
VR2	2	Pin 3 of 10K Ω resistor pot (see Note 1)	-
CNT	3	Connect to toggle switch, one side VCC and other side GND	
GND	4	23	GND
GND	5	26	GND
VIN	6	2	+12VSAFE
VIN	7	2	+12VSAFE

Interfacing to the Toshiba LTM12C016 Panel

Panel General Description:

Resolution:	1024 x 768	Display Color:	262,144 colors
Type:	Color TFT	Display Area:	247 x 184 mm
Pixel Depth:	18 bits/pixel	Pixel/SHFCLK:	2

- Uses 5.0V power supply technology
- Set XVCC and DVCC to 5.0V.

Panel Connector Interfaces

CN2 Connector

Chips DK55X		Toshiba Connector	
Pin name	Pin #	Pin #	Pin Name
GND	12	1	GND
SHFCLK	13	2	CLK
GND	14	3	GND
P23	49	4	RE5
P22	48	5	RE4
P21	46	6	RE3
P20	45	7	RE2
GND	41	8	RE1
GND	41	9	RE0
GND	47	10	GND

CN3 Connector

Chips DK55X		Toshiba Connector	
Pin name	Pin #	Pin #	Pin Name
GND	47	1	GND
P19	43	2	RO5
P18	42	3	RO4
P17	40	4	RO3
P16	39	5	RO2
GND	44	6	RO1
GND	44	7	RO0
GND	44	8	GND
P15	37	9	GE5
P14	36	10	GE4
P13	34	11	GE3
P12	33	12	GE2
GND	29	13	GE1
GND	29	14	GE0
GND	29	15	GND

Panel Connector Interfaces (continued)**CN4 Connector**

Chips DK55X		Toshiba Connector	
Pin name	Pin #	Pin #	Pin Name
GND	29	1	GND
P11	31	2	GO5
P10	30	3	GO4
P9	28	4	GO3
P8	27	5	GO2
GND	35	6	GO1
GND	20	7	GO0
GND	20	8	GND
P15	25	9	BE5
P14	24	10	BE4
P13	22	11	BE3
P12	21	12	BE2
GND	14	13	BE1
GND	26	14	BE0
GND	26	15	GND

CN5 Connector

Chips DK55X		Toshiba Connector	
Pin name	Pin #	Pin #	Pin Name
P11	19	1	BO5
P10	18	2	BO4
P1	16	3	BO3
P0	15	4	BO3
GND	20	5	BO1
GND	20	6	BO0
VDDsafe	1	7	VDD
VDDsafe	1	8	VDD
VDDsafe	1	9	VDD
DE	8	10	ENAB

Register Information

Control Register		FP Mode Registers		SM mode Registers	
FR03	08	FR21	82	FR21	82
FR08	0C	FR22	13	FR22	13
FR0A	08	FR23	A3	FR23	A3
FR18	00	FR20	7F	FR20	7F
FR1E	80	FR34	00	FR34	00
FR40	1F	FR24	81	FR24	81
FR41	03	FR25	00	FR25	00
FR48	13	FR27	10	FR27	10
FR4D	40	FR26	00	FR26	00
FR4E	3F	FR37	80	FR37	80
FR50	00	FR33	24	FR33	24
		FR35	32	FR35	32
		FR36	03	FR36	03
		FR31	02	FR31	02
		FR32	08	FR32	08
		FR30	FF	FR30	FF
		FR10	1C	FR10	1C
		FR11	D2	FR11	D2
		FR12	50	FR12	50
		FR13	00	FR13	00
		FR16	03	FR16	03
		FR17	BD	FR17	BD
		FR1A	00	FR1A	00

Interfacing to the Sharp LQ14X01 Panel

Panel General Description:

Resolution: 1024 x 768
 Type: Color TFT LCD
 Pixel Depth: 2 x 18 bits/pixel

Display Color: 262,144 color
 Diagonal Length: 13.8"
 Pixel/SHFCLK: 2

- Uses 5.0V power supply technology
- Latches data on the rising edge of the shift clock

Panel Connector Interface

Chips DK 55X connector		Sharp Connector	
Pin name	Pin #	Pin #	Pin Name
J11 - 13	GND	1	GND
J11 - 14	P30	2	RB0
J11 - 16	P31	3	RB1
J11 - 18	P32	4	RB2
J11 - 20	P33	5	RB3
J11 - 22	P34	6	RB4
J11 - 24	P35	7	RB5
J11 - 26	GND	8	GND
42	P18	9	GB0
43	P19	10	GB1
45	P20	11	GB2
46	P21	12	GB3
48	P22	13	GB4
49	P23	14	GB5
50	GND	15	GND
24	P6	16	BB0
25	P7	17	BB1
27	P8	18	BB2
28	P9	19	BB3
30	P10	20	BB4
31	P11	21	BB5
J11 - 1	GND	22	GND
J11 - 2	P24	23	RA0
J11 - 4	P25	24	RA1
J11 - 6	P26	25	RA2
J11 - 8	P27	26	RA3
J11 - 10	P28	27	RA4
J11 - 12	P29	28	RA5
J11 - 19	GND	29	GND
33	P12	30	GA0
34	P13	31	GA1
36	P14	32	GA2
37	P15	33	GA3
39	P16	34	GA4
40	P17	35	GA5

Panel Connector Interface (continued)

Chips DK 55X connector		Sharp Connector	
Pin name	Pin #	Pin #	Pin Name
38	GND	36	GND
15	P0	37	BA0
16	P1	38	BA1
18	P2	39	BA2
19	P3	40	BA3
21	P4	41	BA4
22	P5	42	BA5
23	GND	43	GND
26	GND	44	REV1
29	GND	45	GND
11	FLM	46	VSYNC
10	LP	47	HSYNC
8	DE	48	DE
17	GND	49	GND
20	GND	50	GND
13	SHFCLK	51	CKB
13	SHFCLK	52	CKA
6	GND	53	GND
9	GND	54	GND
12	GND	55	REV2
14	GND	56	REV3
1	VDDSAFE(5V)	57	VCC
1	VDDSAFE(5V)	58	VCC
1	VDDSAFE(5V)	59	VCC
1	VDDSAFE(5V)	60	VCC

Register Information

Control Register		FP Mode registers		SM mode registers	
FR03	08	FR21	82	FR21	82
FR08	08	FR22	13	FR22	13
FR0A	0C	FR23	A3	FR23	A3
FR18	00	FR20	7F	FR20	7F
FR1E	80	FR34	00	FR34	00
FR40	1F	FR24	81	FR24	81
FR41	03	FR25	00	FR25	00
FR48	13	FR27	10	FR27	10
FR4D	40	FR26	00	FR26	00
FR4E	3F	FR37	9A	FR37	9A
FR50	00	FR33	24	FR33	24
		FR35	32	FR35	32
		FR36	03	FR36	03
		FR31	02	FR31	02
		FR32	08	FR32	08
		FR30	FF	FR30	FF
		FR10	0C	FR10	0C
		FR11	E0	FR11	E0
		FR12	D0	FR12	D0
		FR13	00	FR13	00
		FR16	03	FR16	03
		FR17	BD	FR17	BD
		FR1A	00	FR1A	00

Interfacing to the Hitachi D01VC1CAA Panel

Panel General Description:

Resolution:	1024 x 768	Display Color:	262,144 colors
Type:	Color TFT LCD	Display Area:	245.8 x 184.3 mm
Pixel Depth:	2 x 18 bits/pixel	Pixel/SHFCLK:	2

- Uses 3.3V power supply technology
- Set XVCC and DVCC to 3.3V.
- LP and FLM polarity are negative

Panel Connector Interface

Chips DK 55X connector		Hitachi Connector	
Pin name	Pin #	Pin #	Pin Name
VSS	1 (J11)	1	VSS
SHFCLK	13 (J5)	2	DCLK
VSS	3 (J11)	3	VSS
LP	10 (J5)	4	HSYNC
FLM	11 (J5)	5	VSYN
VSS	5 (J11)	6	VSS
R00 (P24)	2 (J11)	7	RA0
R10 (P30)	14 (J11)	8	RB0
VSS	7 (J11)	9	VSS
R01 (P25)	4 (J11)	10	RA1
R11 (P31)	16 (J11)	11	RB1
VSS	9 (J11)	12	VSS
R02 (P26)	6 (J11)	13	RA2
R12 (P32)	18 (J11)	14	RB2
VSS	11 (J11)	15	VSS
R03 (P27)	8 (J11)	16	RA3
R13 (P33)	20 (J11)	17	RB3
VSS	13 (J11)	18	VSS
R04 (P28)	10 (J11)	19	RA4
R14 (P34)	22 (J11)	20	RB4
VSS	15 (J11)	21	VSS
R05 (P29)	12 (J11)	22	RA5
R15 (P35)	24 (J11)	23	RB5
VSS	17 (J11)	24	VSS
G00 (P12)	33 (J5)	25	GA0
G10 (P18)	42 (J5)	26	GB0
VSS	32 (J5)	27	VSS
G01 (P13)	34 (J5)	28	GA1
G11 (P19)	43 (J5)	29	GB1
VSS	32 (J5)	30	VSS
G02 (P14)	36 (J5)	31	GA2
G12 (P20)	45 (J5)	32	GB2
VSS	35 (J5)	33	VSS
G03 (P15)	37 (J5)	34	GA3
G13 (P21)	46 (J5)	35	GB3

Panel Connector Interface (continued)

Chips DK 55X connector		Hitachi Connector	
Pin name	Pin #	Pin #	Pin Name
VSS	35 (J5)	36	VSS
G04 (P16)	39 (J5)	37	GA4
G14 (P22)	48 (J5)	38	GB4
VSS	38 (J5)	39	VSS
G05 (P17)	40 (J5)	40	GA5
G15 (P23)	49 (J5)	41	GB5
VSS	38 (J5)	42	VSS
B00 (P0)	15 (J5)	43	BA0
B10 (P6)	24 (J5)	44	BB0
VSS	6 (J5)	45	VSS
B01 (P1)	16 (J5)	46	BA1
B11 (P7)	25 (J5)	47	BB1
VSS	6 (J5)	48	VSS
B02 (P2)	18 (J5)	49	BA2
B12 (P8)	27 (J5)	50	BB2
VSS	9 (J5)	51	VSS
B03 (P3)	19 (J5)	52	BA3
B13 (P9)	28 (J5)	53	BB3
VSS	9 (J5)	54	VSS
B04 (P4)	21 (J5)	55	BA4
B14 (P10)	30 (J5)	56	BB4
VSS	12 (J5)	57	VSS
B05 (P5)	22 (J5)	58	BA5
B15 (P11)	31 (J5)	59	BB5
VSS	12 (J5)	60	VSS
M (DE)	7 (J5)	61	DTMG
VSS	14 (J5)	62	VSS
VSS	17 (J5)	63	INV
-	-	64	NC
DVCC55X	4 (J5)	65	VDD (3.3V)
DVCC55X	4 (J5)	66	VDD (3.3V)
DVCC55X	4 (J5)	67	VDD (3.3V)
DVCC55X	4 (J5)	68	VDD (3.3V)
-	-	69	NC
-	-	70	NC

Register Information

Control Register		FP Mode registers		SM mode registers	
FR03	08	FR21	82	FR21	82
FR08	0C	FR22	13	FR22	13
FR0A	08	FR23	A3	FR23	A3
FR18	00	FR20	7F	FR20	7F
FR1E	80	FR34	00	FR34	00
FR40	1F	FR24	81	FR24	81
FR41	03	FR25	00	FR25	00
FR48	13	FR27	10	FR27	10
FR4D	40	FR26	00	FR26	00
FR4E	3F	FR37	80	FR37	80
FR50	00	FR33	24	FR33	24
		FR35	32	FR35	32
		FR36	03	FR36	03
		FR31	02	FR31	02
		FR32	08	FR32	08
		FR30	FF	FR30	FF
		FR10	0C	FR10	0C
		FR11	E4	FR11	E4
		FR12	D0	FR12	D0
		FR13	00	FR13	00
		FR16	03	FR16	03
		FR17	BD	FR17	BD
		FR1A	00	FR1A	00

Interfacing to the Fujitsu FLC31SVC6S Panel

Panel General Description:

Resolution: 800 x 600
 Type: Color TFT
 Pixel Depth: 18 bits/pixel

Display Color: 262,144 colors
 Display Area: 257 x 199 mm
 Pixel/SHFCLK: 1

- Uses 3.3V power supply technology
- Set XVCC and DVCC to 3.3V.
- LP and FLM polarity are negative

Panel Connector Interfaces

CN3: MOLEX 51021-1500

Chips DK55X		Fujitsu Connector	
Pin name	Pin #	Pin #	Pin Name
P15	37	1	G5
P14	36	2	G4
P13	34	3	G3
GND	32	4	GND
P12	33	5	G2
P11	31	6	G1
P10	30	7	G0
GND	38	8	GND
P23	49	9	R5
P22	48	10	R4
P21	46	11	R3
GND	47	12	GND
P20	45	13	R2
P19	43	14	R1
P18	42	15	R0

CN4: MOLEX 51021-1400

Chips DK55X		Fujitsu Connector	
Pin name	Pin #	Pin #	Pin Name
FLM	11	1	VSYNC
LP	10	2	HSYNC
GND	12	3	GND
SHFCLK	13	4	CLK
GND	14	5	GND
DE	8	6	ENAB
GND	6	7	GND
P7	25	8	B5
P6	24	9	B4
P5	22	10	B3
GND	20	11	GND
P4	21	12	B2
P3	19	13	B1
P2	18	14	B0

CN2: MOLEX 51021-0500

Chips DK55X		Fujitsu Connector	
Pin name	Pin #	Pin #	Pin Name
GND	41	1	GND
GND	29	2	GND
GND	17	3	GND
VCC	4	4	VCC
VCC	4	5	VCC
VDDsafe	1	39	VCC
VDDsafe	1	40	VCC
N/C	--	41	NC

Register Information

Control Register		FP Mode registers		SM mode registers	
FR06	C0	FR19	6B	FR19	6B
FR0F	10	FR1A	1B	FR1A	1B
FR4F	46	FR1B	7F	FR1B	7F
FR50	88	FR1C	63	FR1C	63
FR51	C4	FR2C	00	FR2C	00
FR54	F8	FR2D	68	FR2D	68
FR55	F3	FR2E	68	FR2E	68
FR56	00	FR2F	0F	FR2F	0F
FR57	23	FR53	0C	FR53	0C
FR5B	81	FR50	08	FR50	08
FR5D	10	FR64	72	FR64	72
FR5E	80	FR65	E0	FR65	E0
FR6C	08	FR66	58	FR66	58
FR6E	BD	FR67	0C	FR67	0C
FR6F	00	FR68	57	FR68	57
FR44	07	FR6F	00	FR6F	00
FR59	04	FR5F	0F	FR5F	0F
FR5A	02				

Interfacing to the Samsung LT121-103 Panel

Panel General Description:

Resolution: 800 x 600
 Type: Color TFT LCD
 Bit/pixel: 18

Display Color: 262,144 color
 Diagonal Length: 12.1"
 Pixel/SHFCLK: 1

Panel Connector Interface

Chips DK 55X connector		Samsung connector	
Pin name	Pin #	Pin #	Pin Name
GND	9	1	GND
SHFCLK	13	2	DCLK
GND	12	3	GND
LP	10	4	HSYNC
FLM	11	5	VSYNC
GND	14	6	GND
GND	17	7	GND
GND	20	8	GND
P18	42	9	R0
P19	43	10	R1
P20	45	11	R2
GND	23	12	GND
P21	46	13	R3
P22	48	14	R4
P23	49	15	R5
GND	26	16	GND
GND	29	17	GND
GND	32	18	GND
P10	30	19	G0
P11	31	20	G1
P12	33	21	G2
GND	35	22	GND
P13	34	23	G3
P14	36	24	G4
P15	37	25	G5
GND	38	26	GND
GND	41	27	GND
GND	44	28	GND
P10	18	29	B0
P11	19	30	B1
P12	21	31	B2
GND	47	32	GND
P13	22	33	B3
P14	24	34	B4
P15	25	35	B5
GND	50	36	GND
DE	8	37	DE
N/C	--	38	NC
VDDsafe	1	39	VCC
VDDsafe	1	40	VCC
N/C	--	41	NC

Register Information

Control Register		FP Mode registers		SM mode registers	
FR03	08	FR21	68	FR21	68
FR08	0C	FR22	18	FR22	18
FR0A	0C	FR23	7F	FR23	7F
FR18	00	FR20	63	FR20	63
FR1E	80	FR34	00	FR34	00
FR40	1F	FR24	67	FR24	67
FR41	03	FR25	00	FR25	00
FR48	13	FR27	0F	FR27	0F
FR4D	50	FR26	00	FR26	00
FR4E	3F	FR37	80	FR37	80
FR50	00	FR33	72	FR33	72
		FR35	22	FR35	22
		FR36	02	FR36	02
		FR31	58	FR31	58
		FR32	0C	FR32	0C
		FR30	57	FR30	57
		FR10	0C	FR10	0C
		FR11	E0	FR11	E0
		FR12	50	FR12	50
		FR13	00	FR13	00
		FR16	03	FR16	03
		FR17	BD	FR17	BD
		FR1A	00	FR1A	00

Unique Panel Features:

- Uses 3.3V power supply technology
- Set XVCC and DVCC to 3.3V.
- LP and FLM polarity are negative

Interfacing to the Optrex DMF-50714NCU-FW Panel

Panel General Description:

Resolution:	1024x768	Display Color:	256k
Type:	DSTN 16-bit	Diagonal Length:	TBD
Bit/pixel:	3 bits/pixel	Pixel/SHFCLK:	5(4 -bit packed)

- Uses 5.0V power supply technology
- 16-bit Interface, 4-bit packed
- LP and FLM polarity are positive

Panel Connector Interface

CN1:

Molex 53261-1510			
Chips DK 55X connector		Optrex connector	
Pin Name	Pin #	Pin #	Pin Name
FLM	11	1	FLM
GND	6	2	VSS
-	*	3	DISP_OFF
LP	10	4	CL1
GND	9	5	VSS
SHFCLK	13	6	CL2
GND	12	7	VSS
UG2 (P11)	31	8	UD0
UR2 (P10)	30	9	UD1
UB1 (P9)	28	10	UD2
UG1 (P8)	27	11	UD3
UR1 (P3)	19	12	UD4
UB0 (P2)	18	13	UD5
UG0 (P1)	16	14	UD6
UR0 (P0)	15	15	UD7

* Connect to toggle switch, one side VCC and other side GND.

CN2:

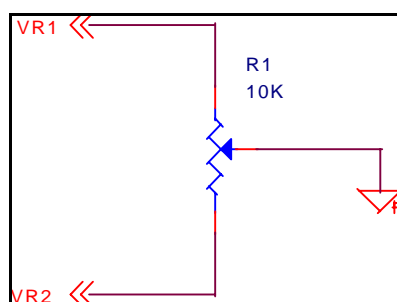
Molex 53261-1410			
Chips DK 55X connector		Optrex connector	
LG2 (P15)	37	1	LD0
LR2 (P14)	36	2	LD1
LB1 (P13)	34	3	LD2
LG1 (P12)	33	4	LD3
LR1 (P7)	25	5	LD4
LB0 (P6)	24	6	LD5
LG0 (P5)	22	7	LD6
LR0 (P4)	21	8	LD7
VDDSAFE	1	9	VDD
VDDSAFE	1	10	VDD
GND	14	11	VSS
VEESAFE*	3	12	VR
	NC	13	NC
	NC	14	NC

* Typical: +32V

CN3:

Molex 53261-0710			
Chips DK 55X connector		Optrex connector	
-	†	1	VR1
-	††	2	VR2
	‡	3	CNT
GND	23	4	GND
GND	26	5	GND
+12VSAFE	2	6	VIN
+12VSAFE	2	7	VIN

- † Pin 1 of 10K Ω resistor pot (see schematic at right)
 †† Pin 3 of 10K Ω resistor pot (see schematic at right)
 ‡ Connect to toggle switch, one side VCC and other side GND



Register Information

Control Register		FP Mode registers		SM mode registers	
FR03	08	FR21	83	FR21	83
FR08	00	FR22	14	FR22	14
FR0A	08	FR23	A3	FR23	A3
FR18	00	FR20	7F	FR20	7F
FR1E	80	FR34	23	FR34	23
FR40	1F	FR24	00	FR24	00
FR41	03	FR25	00	FR25	00
FR48	17	FR27	10	FR27	10
FR4D	40	FR26	10	FR26	10
FR4E	3C	FR37	00	FR37	00
FR50	00	FR33	23	FR33	23
		FR35	32	FR35	32
		FR36	03	FR36	03
		FR31	01	FR31	01
		FR32	08	FR32	08
		FR30	FF	FR30	FF
		FR10	2F	FR10	2F
		FR11	D5	FR11	D5
		FR12	0E	FR12	0E
		FR13	05	FR13	05
		FR16	03	FR16	03
		FR17	BD	FR17	BD
		FR1A	19	FR1A	19

Interfacing to the Hitachi LMG9972ZWCC Panel

Panel General Description:

Resolution:	800 x 600	Display Color:	262,144 colors
Type:	Color STN-DD	Display Area:	245.8 x 184.3 mm
Pixel Depth:	16 bits/pixel	Pixel/SHFCLK:	1

Panel Connector Interface

Chips DK 55X connector		Hitachi Connector	
Pin name	Pin #	Pin #	Pin Name
P7	25	1	LD4 (LR2)
GND	6	2	VSS GND
P6	24	3	LD5 (LB1)
FLM	11	4	FLM FLM
P5	22	5	LD6 (LG1)
LP	10	6	CL1-LP
P4	21	7	LD7 (LR1)
GND	12	8	VSS-GND
GND	14	9	VSS-GND
SHFCLK	13	10	CL2-SHFCLK
P15	37	11	LD0 (LG3)
External Source	†	12	VCON typical 0.0V-6.0V
P14	36	13	LD1 (LR3)
VDD SAFE	1	14	VDD
GND	17	15	VSS-GND
VDD SAFE	1	16	VDD
P13	34	17	LD2 (LB2)
VDD SAFE	††	18	DISP 5.0V -> ON, 0.0 V -> OFF
P12	33	19	LD3 (LG2)
		20	NC
GND	20	21	VSS-GND
P8	27	22	UD3 (UG2)
P3	19	23	UD4 (UR2)
P9	28	24	UD2 (UB2)
P2	18	25	UD5 (UB1)
P10	30	26	UD1 (UR3)
GND	23	27	VSS-GND
P11	31	28	UD0 (UG3)
P1	16	29	UD6 (UG1)
GND	26	30	VSS GND
P0	15	31	UD7 (UR1)

† Use a wire to connect this pin to an external power source.

†† Use a switch to control the display.

Register Information

Control Register		FP Mode registers		SM mode registers	
FR03	08	FR21	68	FR21	68
FR08	00	FR22	18	FR22	18
FR0A	08	FR23	7F	FR23	7F
FR18	00	FR20	63	FR20	63
FR1E	80	FR34	1B	FR34	1B
FR40	1F	FR24	70	FR24	70
FR41	03	FR25	00	FR25	00
FR48	13	FR27	0F	FR27	0F
FR4D	50	FR26	00	FR26	00
FR4E	3F	FR37	00	FR37	00
FR50	00	FR33	72	FR33	72
		FR35	22	FR35	22
		FR36	02	FR36	02
		FR31	58	FR31	58
		FR32	0C	FR32	0C
		FR30	57	FR30	57
		FR10	1F	FR10	1F
		FR11	45	FR11	45
		FR12	0E	FR12	0E
		FR13	01	FR13	01
		FR16	03	FR16	03
		FR17	BD	FR17	BD
		FR1A	1B	FR1A	1B

Interfacing to the NEC NL8060BC31-01 Panel

Panel General Description:

Resolution: 800 x 600
 Type: Color TFT
 Pixel Depth: 18 bits/pixel

Display Color: 262,144 colors
 Display Area: 245.8 x 184.3 mm
 Pixel/SHFCLK: 1

Panel Connector Interface

Chips DK 55X connector		NEC Connector	
Pin name	Pin #	Pin #	Pin Name
GND	9	1	GND
SHFCLK	13	2	DCLK
GND	12	3	GND
LP	10	4	HSYNC
FLM	11	5	VSYNC
GND	14	6	GND
GND	17	7	GND
GND	20	8	GND
P18	42	9	R0
P19	43	10	R1
P20	45	11	R2
GND	23	12	GND
P21	46	13	R3
P22	48	14	R4
P23	49	15	R5
GND	26	16	GND
GND	29	17	GND
GND	32	18	GND
P10	30	19	G0
P11	31	20	G1
P12	33	21	G2
GND	35	22	GND
P13	34	23	G3
P14	36	24	G4
P15	37	25	G5
GND	38	26	GND
GND	41	27	GND
GND	44	28	GND
P2	18	29	B0
P3	19	30	B1
P4	21	31	B2
GND	47	32	GND
P5	22	33	B3
P6	24	34	B4
P7	25	35	B5
GND	50	36	GND
DE	8	37	DE
VDDsafe	1	38	VCC
VDDsafe	1	39	VCC
VDDsafe	1	40	VCC
----	N/C	41	MODE

Unique Panel Features:

- LP and FLM polarity are negative

Register Information

Control Register		FP Mode registers		SM mode registers	
FR03	08	FR21	68	FR21	68
FR08	00	FR22	18	FR22	18
FR0A	08	FR23	7F	FR23	7F
FR18	00	FR20	63	FR20	63
FR1E	80	FR34	1B	FR34	00
FR40	1F	FR24	70	FR24	67
FR41	03	FR25	00	FR25	00
FR48	13	FR27	0F	FR27	0F
FR4D	50	FR26	00	FR26	00
FR4E	3F	FR37	00	FR37	80
FR50	00	FR33	72	FR33	72
		FR35	22	FR35	22
		FR36	02	FR36	02
		FR31	58	FR31	58
		FR32	0C	FR32	0C
		FR30	57	FR30	57
		FR10	1F	FR10	0C
		FR11	45	FR11	E0
		FR12	0E	FR12	50
		FR13	01	FR13	00
		FR16	03	FR16	03
		FR17	BD	FR17	BD
		FR1A	00	FR1A	00

Interfacing to the Hitachi TX30D01VC1CAA Panel

Panel General Description:

Resolution:	800 x 600	Display Color:	262,144 colors
Type:	Color TFT	Display Area:	245.8 x 184.3 mm
Pixel Depth:	18 bits/pixel	Pixel/SHFCLK:	1

- Uses 3.3V power supply technology
- Set XVCC and DVCC to 3.3V.

Panel Connector Interface

Chips DK 55X connector		Hitachi Connector	
Pin name	Pin #	Pin #	Pin Name
GND	9	1	VSS
SHFCLK	13	2	DCLK
GND	12	3	VSS
LP	10	4	HSYNC
FLM	11	5	VSYN
GND	14	6	VSS
GND	17	7	VSS
GND	20	8	VSS
P18	42	9	R0
P19	43	10	R1
P20	45	11	R2
GND	23	12	VSS
P21	46	13	R3
P22	48	14	R4
P23	49	15	R5
GND	26	16	VSS
GND	29	17	VSS
GND	32	18	VSS
P10	30	19	G0
P11	31	20	G1
P12	33	21	G2
GND	35	22	VSS
P13	34	23	G3
P14	36	24	G4
P15	37	25	G5
GND	38	26	VSS
GND	41	27	VSS
GND	44	28	VSS
P2	18	29	B0
P3	19	30	B1
P4	21	31	B2
GND	47	32	VSS
P5	22	33	B3
P6	24	34	B4
P7	25	35	B5
GND	50	36	VSS
DE	8	37	DTMG
	N/C	38	N/C
3.3V		39	VDD
3.3V		40	VDD
	N/C	41	IC

Register Information

Control Register		FP Mode registers		SM mode registers	
FR03	08	FR21	68	FR21	68
FR08	00	FR22	18	FR22	18
FR0A	0C	FR23	7F	FR23	7F
FR18	00	FR20	63	FR20	63
FR1E	80	FR34	02	FR34	02
FR40	1F	FR24	67	FR24	67
FR41	03	FR25	00	FR25	00
FR48	13	FR27	0F	FR27	0F
FR4D	50	FR26	00	FR26	00
FR4E	3F	FR37	00	FR37	00
FR50	00	FR33	72	FR33	72
		FR35	22	FR35	22
		FR36	02	FR36	02
		FR31	58	FR31	58
		FR32	0C	FR32	0C
		FR30	57	FR30	57
		FR10	0C	FR10	0C
		FR11	E0	FR11	E0
		FR12	50	FR12	50
		FR13	00	FR13	00
		FR16	03	FR16	03
		FR17	BD	FR17	BD
		FR1A	00	FR1A	00

Interfacing to the Hitachi LMG9970ZWCC Panel

Panel General Description:

Resolution:	800 x 600	Display Color:	262,144 colors
Type:	Color STN-DD	Display Area:	245.8 x 184.3 mm
Pixel Depth:	16 bits/pixel	Pixel/SHFCLK:	1

Panel Connector Interface

Chips DK 55X connector		Hitachi Connector	
Pin name	Pin #	Pin #	Pin Name
P7	25	1	LD4 (LR2)
GND	6	2	VSS GND
P6	24	3	LD5 (LB1)
FLM	11	4	FLM FLM
P5	22	5	LD6 (LG1)
LP	10	6	CL1-LP
P4	21	7	LD7 (LR1)
GND	12	8	VSS-GND
GND	14	9	VSS-GND
SHFCLK	13	10	CL2-SHFCLK
P15	37	11	LD0 (LG3)
External Source	†	12	VCON typical 0.0V-6.0V
P14	36	13	LD1 (LR3)
VDD SAFE	1	14	VDD
GND	17	15	VSS-GND
VDD SAFE	1	16	VDD
P13	34	17	LD2 (LB2)
VDD SAFE	††	18	DISP 5.0V -> ON, 0.0 V -> OFF
P12	33	19	LD3 (LG2)
		20	NC
GND	20	21	VSS-GND
P8	27	22	UD3 (UG2)
P3	19	23	UD4 (UR2)
P9	28	24	UD2 (UB2)
P2	18	25	UD5 (UB1)
P10	30	26	UD1 (UR3)
GND	23	27	VSS-GND
P11	31	28	UD0 (UG3)
P1	16	29	UD6 (UG1)
GND	26	30	VSS GND
P0	15	31	UD7 (UR1)

† Use a wire to connect this pin to an external power source.

†† Use a switch to control the display.

Register Information

Control Register		FP Mode registers		SM mode registers	
FR03	08	FR21	68	FR21	68
FR08	00	FR22	18	FR22	18
FR0A	08	FR23	7F	FR23	7F
FR18	00	FR20	63	FR20	63
FR1E	80	FR34	1B	FR34	1B
FR40	1F	FR24	70	FR24	70
FR41	03	FR25	00	FR25	00
FR48	13	FR27	0F	FR27	0F
FR4D	50	FR26	00	FR26	00
FR4E	3F	FR37	00	FR37	00
FR50	00	FR33	72	FR33	72
		FR35	22	FR35	22
		FR36	02	FR36	02
		FR31	58	FR31	58
		FR32	0C	FR32	0C
		FR30	57	FR30	57
		FR10	1F	FR10	1F
		FR11	45	FR11	45
		FR12	0E	FR12	0E
		FR13	01	FR13	01
		FR16	03	FR16	03
		FR17	BD	FR17	BD
		FR1A	1B	FR1A	1B

Interfacing to the Sharp LM15X80 XGA DSTN Panel

Panel General Description:

Resolution:	1024 x 768	Display Color:	N/A
Type:	XGA DSTN	Display Area:	309x233mm
Pixel Depth:	3 bits/pixel	Pixel/SHFCLK:	8

Panel Connector Interface

Chips DK 55X connector	Sharp Connector		
Pin Name	Pin #	Pin #	Pin Name
VSS	6	1	VSS
VSS	9	2	VSS
SHFCLK	13	3	XCK
VSS	12	4	VSS
VSS	14	5	VSS
†	—	6	VCON
LP	10	7	LP
VDDSAFE	1	8	VDD
FLM	11	9	YD
VDDSAFE	1	10	VDD
VSS	17	11	VSS
VSS	20	12	VSS
‡	—	13	DISP
VSS	23	14	VSS
LR0 (P3)	19	15	DL11
UR0 (P0)	15	16	DU11
LG0 (P4)	21	17	DL10
UG0 (P1)	16	18	DU10
LB0 (P5)	22	19	DL9
UB0 (P2)	18	20	DU9
LR1 (P9)	28	21	DL8
UR1 (P6)	24	22	DU8
LG1 (P10)	30	23	DL7
UG1 (P7)	25	24	DU7
LB1 (P11)	31	25	DL6
UB1 (P8)	27	26	DU6
LR2 (P15)	37	27	DL5
UR2 (P12)	33	28	DU5
LG2 (P16)	39	29	DL4
UG2 (P13)	34	30	DU4
LB2 (P17)	40	31	DL3
UB2 (P14)	36	32	DU3
LR3 (P21)	46	33	DL2
UR3 (P18)	42	34	DU2
LG3 (P22)	48	35	DL1
UG3 (P19)	43	36	DU1
LB3 (P23)	49	37	DL0
UB3 (P20)	45	38	DU0
VSS	26	39	VSS
VSS	29	40	VSS

† Connect to a resistor pot. Typical: 0V-5V.

‡ Connect to toggle switch:

One side to VDDSAFE and the other to GND.

ON = 5.0V OFF = 0.0V

Register Information

Control Register		FP Mode registers		SM mode registers	
FR03	08	FR21	80	FR21	83
FR08	00	FR22	01	FR22	14
FR0A	08	FR23	85	FR23	A3
FR18	00	FR20	7F	FR20	7F
FR1E	80	FR34	1C	FR34	1A
FR40	1F	FR24	82	FR24	82
FR41	03	FR25	00	FR25	00
FR48	17	FR27	02	FR27	10
FR4D	40	FR26	00	FR26	00
FR4E	33	FR37	00	FR37	00
FR50	00	FR33	1B	FR33	1B
FR16	02	FR35	32	FR35	32
		FR36	03	FR36	03
		FR31	00	FR31	02
		FR32	01	FR32	08
		FR30	FF	FR30	FF
		FR10	2F	FR10	2F
		FR11	C5	FR11	C5
		FR12	56	FR12	56
		FR13	00	FR13	00
		FR16	02	FR16	02
		FR17	BD	FR17	BD
		FR1A	1B	FR1A	1B

Interfacing to the Sanyo LM-GK53-22NTX DSTN Panel

Panel General Description:

Resolution:	1024 x 768	Display Color:	N/A
Type:	XGA DSTN	Display Area:	276.5 x 207.4 mm
Pixel Depth:	3 bits/pixel	Pixel/SHFCLK:	8

Panel Connector Interface

Chips DK 55X connector		Sharp Connector	
Pin Name	Pin #	Pin #	Pin Name
VSS	6	1	VSS
VSS	9	2	VSS
SHFCLK	13	3	XCK
VSS	12	4	VSS
VSS	14	5	VSS
†	—	6	VCON
LP	10	7	LP
VDDSAFE	1	8	VDD
FLM	11	9	YD
VDDSAFE	1	10	VDD
VSS	17	11	VSS
VSS	20	12	VSS
‡	—	13	DISP
VSS	23	14	VSS
LR0 (P3)	19	15	DL11
UR0 (P0)	15	16	DU11
LG0 (P4)	21	17	DL10
UG0 (P1)	16	18	DU10
LB0 (P5)	22	19	DL9
UB0 (P2)	18	20	DU9
LR1 (P9)	28	21	DL8
UR1 (P6)	24	22	DU8
LG1 (P10)	30	23	DL7
UG1 (P7)	25	24	DU7
LB1 (P11)	31	25	DL6
UB1 (P8)	27	26	DU6
LR2 (P15)	37	27	DL5
UR2 (P12)	33	28	DU5
LG2 (P16)	39	29	DL4
UG2 (P13)	34	30	DU4
LB2 (P17)	40	31	DL3
UB2 (P14)	36	32	DU3
LR3 (P21)	46	33	DL2
UR3 (P18)	42	34	DU2
LG3 (P22)	48	35	DL1
UG3 (P19)	43	36	DU1
LB3 (P23)	49	37	DL0
UB3 (P20)	45	38	DU0
VSS	26	39	VSS
VSS	29	40	VSS

† Connect to a resistor pot. Typical: 0V-5V.

‡ Connect to toggle switch:

One side to VDDSAFE and the other to GND.

ON = 5.0V OFF = 0.0V

Register Information

Control Register		FP Mode registers		SM mode registers	
FR03	08	FR21	80	FR21	83
FR08	00	FR22	01	FR22	14
FR0A	08	FR23	85	FR23	A3
FR18	00	FR20	7F	FR20	7F
FR1E	80	FR34	1C	FR34	1A
FR40	1F	FR24	82	FR24	82
FR41	03	FR25	00	FR25	00
FR48	17	FR27	02	FR27	10
FR4D	40	FR26	00	FR26	00
FR4E	33	FR37	00	FR37	00
FR50	00	FR33	1B	FR33	1B
FR16	02	FR35	32	FR35	32
		FR36	03	FR36	03
		FR31	00	FR31	02
		FR32	01	FR32	08
		FR30	FF	FR30	FF
		FR10	2F	FR10	2F
		FR11	C5	FR11	C5
		FR12	56	FR12	56
		FR13	00	FR13	00
		FR16	02	FR16	02
		FR17	BD	FR17	BD
		FR1A	1B	FR1A	1B

Interfacing to the Fujitsu FLC31SVC6S Panel

Panel General Description:

Resolution: 800 x 600
 Type: Color TFT
 Pixel Depth: 18 bits/pixel

Display Color: 262,144 colors
 Display Area: 257 x 199 mm
 Pixel/SHFCLK: 1

- Uses 3.3V power supply technology
- Set XVCC and DVCC to 3.3V.
- LP and FLM polarity are negative

Panel Connector Interfaces

CN3: MOLEX 51021-1500

Chips DK55X		Fujitsu Connector	
Pin name	Pin #	Pin #	Pin Name
P15	37	1	G5
P14	36	2	G4
P13	34	3	G3
GND	32	4	GND
P12	33	5	G2
P11	31	6	G1
P10	30	7	G0
GND	38	8	GND
P23	49	9	R5
P22	48	10	R4
P21	46	11	R3
GND	47	12	GND
P20	45	13	R2
P19	43	14	R1
P18	42	15	R0

CN4: MOLEX 51021-1400

Chips DK55X		Fujitsu Connector	
Pin name	Pin #	Pin #	Pin Name
FLM	11	1	VSYN
LP	10	2	HSYN
GND	12	3	GND
SHFCLK	13	4	CLK
GND	14	5	GND
DE	8	6	ENAB
GND	6	7	GND
P7	25	8	B5
P6	24	9	B4
P5	22	10	B3
GND	20	11	GND
P4	21	12	B2
P3	19	13	B1
P2	18	14	B0

CN2: MOLEX 51021-0500

Chips DK55X		Fujitsu Connector	
Pin name	Pin #	Pin #	Pin Name
GND	41	1	GND
GND	29	2	GND
GND	17	3	GND
VCC	4	4	VCC
VCC	4	5	VCC
VDDsafe	1	39	VCC
VDDsafe	1	40	VCC
N/C	--	41	NC

Register Information

Control Register		FP Mode registers		SM mode registers	
FR06	C0	FR19	6B	FR19	6B
FR0F	10	FR1A	1B	FR1A	1B
FR4F	46	FR1B	7F	FR1B	7F
FR50	88	FR1C	63	FR1C	63
FR51	C4	FR2C	00	FR2C	00
FR54	F8	FR2D	68	FR2D	68
FR55	F3	FR2E	68	FR2E	68
FR56	00	FR2F	0F	FR2F	0F
FR57	23	FR53	0C	FR53	0C
FR5B	81	FR50	08	FR50	08
FR5D	10	FR64	72	FR64	72
FR5E	80	FR65	E0	FR65	E0
FR6C	08	FR66	58	FR66	58
FR6E	BD	FR67	0C	FR67	0C
FR6F	00	FR68	57	FR68	57
FR44	07	FR6F	00	FR6F	00
FR59	04	FR5F	0F	FR5F	0F
FR5A	02				

Interfacing to the Hitachi LMG9970ZWCC Panel

Hitachi LMG9970ZWCC Connection to Chips Flat Panel Connector

Panel Pin Number	DK Board Connector Pin #	Hitachi's name - Chips' name
1	25	LD4 - P7 (LR2)
2	6	VSS - GND
3	24	LD5 - P6 (LB1)
4	11	FLM - FLM
5	22	LD6 - P5 (LG1)
6	10	CL1 - LP
7	21	LD7 - P4 (LR1)
8	12	VSS - GND
9	14	VSS - GND
10	13	CL2 - SHFCLK
11	37	LD0 - P15 (LG3)
12	WIRE TO EXTERNAL POWER SOURCE	VCON typical 0.0V - 6.0V
13	36	LD1 - P14 (LR3)
14	1	VDD
15	17	VSS - GND
16	1	VDD
17	34	LD2 - P13 (LB2)
18	WIRE TO EXTERNAL POWER SOURCE	DISP 5.0V -> ON, 0.0 V -> OFF
19	33	LD3 - P12 (LG2)
20		NC
21	20	VSS - GND
22	27	UD3 - P8 (UG2)
23	19	UD4 - P3 (UR2)
24	28	UD2 - P9 (UB2)
25	18	UD5 - P2 (UB1)
26	30	UD1 - P10 (UR3)
27	23	VSS - GND
28	31	UD0 - P11 (UG3)
29	16	UD6 - P1 (UG1)
30	26	VSS - GND
31	15	UD7 - P0 (UR1)

Interfacing to the Hitachi TX31 D01VC1CAA Panel

Hitachi TX31D01VC1CAA 1024X768 36-BIT TFT PANEL INTERFACE

Panel Pin Name	Panel Pin Number	DK Board Pin Number	Chips Pin Name
VSS	1	1 (J11)	VSS
DCLK	2	13 (J5)	SHFCLK
VSS	3	3 (J11)	VSS
HSYNC	4	10 (J5)	LP
VSYNC	5	11 (J5)	FLM
VSS	6	5 (J11)	VSS
RA0	7	2 (J11)	R00 (P24)
RB0	8	14 (J11)	R10 (P30)
VSS	9	7 (J11)	VSS
RA1	10	4 (J11)	R01 (P25)
RB1	11	16 (J11)	R11 (P31)
VSS	12	9 (J11)	VSS
RA2	13	6 (J11)	R02 (P26)
RB2	14	18 (J11)	R12 (P32)
VSS	15	11 (J11)	VSS
RA3	16	8 (J11)	R03 (P27)
RB3	17	20 (J11)	R13 (P33)
VSS	18	13 (J11)	VSS
RA4	19	10 (J11)	R04 (P28)
RB4	20	22 (J11)	R14 (P34)
VSS	21	15 (J11)	VSS
RA5	22	12 (J11)	R05 (P29)
RB5	23	24 (J11)	R15 (P35)
VSS	24	17 (J11)	VSS
GA0	25	33 (J5)	G00 (P12)
GB0	26	42 (J5)	G10 (P18)
VSS	27	32 (J5)	VSS
GA1	28	34 (J5)	G01 (P13)
GB1	29	43 (J5)	G11 (P19)
VSS	30	32 (J5)	VSS
GA2	31	36 (J5)	G02 (P14)
GB2	32	45 (J5)	G12 (P20)
VSS	33	35 (J5)	VSS
GA3	34	37 (J5)	G03 (P15)
GB3	35	46 (J5)	G13 (P21)

Hitachi TX31D01VC1CAA 1024X768 36-BIT TFT PANEL INTERFACE(continued)

Panel Pin Name	Panel Pin Number	DK Board Pin Number	Chips Pin Name
VSS	36	35 (J5)	VSS
GA4	37	39 (J5)	G04 (P16)
GB4	38	48 (J5)	G14 (P22)
VSS	39	38 (J5)	VSS
GA5	40	40 (J5)	G05 (P17)
GB5	41	49 (J5)	G15 (P23)
VSS	42	38 (J5)	VSS
BA0	43	15 (J5)	B00 (P0)
BB0	44	24 (J5)	B10 (P6)
VSS	45	6 (J5)	VSS
BA1	46	16 (J5)	B01 (P1)
BB1	47	25 (J5)	B11 (P7)
VSS	48	6 (J5)	VSS
BA2	49	18 (J5)	B02 (P2)
BB2	50	27 (J5)	B12 (P8)
VSS	51	9 (J5)	VSS
BA3	52	19 (J5)	B03 (P3)
BB3	53	28 (J5)	B13 (P9)
VSS	54	9 (J5)	VSS
BA4	55	21 (J5)	B04 (P4)
BB4	56	30 (J5)	B14 (P10)
VSS	57	12 (J5)	VSS
BA5	58	22 (J5)	B05 (P5)
BB5	59	31 (J5)	B15 (P11)
VSS	60	12 (J5)	VSS
DTMG	61	7 (J5)	M (DE)
VSS	62	14 (J5)	VSS
INV	63	17 (J5)	VSS
NC	64	-	-
VDD (3.3V)	65	4 (J5)	DVCC55X
VDD (3.3V)	66	4 (J5)	DVCC55X
VDD (3.3V)	67	4 (J5)	DVCC55X
VDD (3.3V)	68	4 (J5)	DVCC55X
NC	69	-	-
NC	70	-	-

Interfacing 6555x with a Sanyo LM-GD53-22NAZ

Panel General Description:

Resolution: 1024 x 768
 Type: 12.1" XGA DSTN
 Pixel Depth: 3 bits/pixel

Panel Voltage range: 3-5.5 volts
 Pixel/SHFCLK: 8

Panel Connector Interfaces

DK6555x Connector		Sanyo Panel Connector	
Pin Name	Pin #	Pin #	Pin Name
VSS	6	1	VSS(GND)
SHFCLK	13	2	CL2
VSS	9	3	VSS(GND)
VSS	12	4	VSS(GND)
LP	10	5	CL1
FLM	11	6	FLM
VSS	14	7	VSS(GND)
VSS	17	8	VSS(GND)
VDDSAFE	1	9	VDD
*		10	DISPOFF
LR0(P3)	19	11	LD11
LG0(P4)	21	12	LD10
LB0(P5)	22	13	LD9
LR1(P9)	28	14	LD8
LG1(P10)	30	15	LD7
LB1(P11)	31	16	LD6
LR2(P15)	37	17	LD5
LG2(P16)	39	18	LD4
LB2(P17)	40	19	LD3
LR3(P21)	46	20	LD2
LG3(P22)	48	21	LD1
LB3(P23)	49	22	LD0
VSS	20	23	VSS(GND)
UB3(P20)	45	24	UD0
UG3(P19)	43	25	UD1
UR3(P18)	42	26	UD2
UB2(P14)	36	27	UD3
UG2(P13)	34	28	UD4
UR2(P12)	33	29	UD5
UB1(P8)	27	30	UD6
UG1(P7)	25	31	UD7
UR1(P6)	24	32	UD8
UB0(P2)	18	33	UD9
UG0(P1)	16	34	UD10
UR0(P0)	15	35	UD11
VDDSAFE	1	36	VDD
VDDSAFE	1	37	VDD
**		38	Vcon
N/C	-	39	N/C
VSS	26	40	VSS(GND)
VSS	29	41	VSS(GND)

* Can be connected to a switch to switch between GND:OFF and VDDSAFE:ON or just connected to VDDSAFE to keep panel on.

**Connect to resistor pot to be able to achieve variable voltage to Vcon of 8 V-2.8 V.

Interfacing 6555x with a Samsung LT133X1-104

Panel General Description:

Resolution:	1024 x 768	Panel Voltage range:	5 volts
Type:	13.3" XGA TFT	Pixel/SHFCLK:	2
Pixel Depth:	3 bits/pixel	Interface:	18+18 Dual channel 5V LVDS

LVDS transmitter output to Panel 20 pin connector

		Samsung LT133X-104 20 pin connector		
	Pin Name	Pin #	Pin #	Pin Name
LVDS – National DS90CF561 (1st data-Odd chip)	TxOut0-	41	5	R1IN0-
	TxOut0+	40	6	R1IN0+
	TxOut1-	39	7	R1IN1-
	TxOut1+	38	8	R1IN1+
	TxOut2-	35	9	R1IN2-
	TxOut2+	34	10	R1IN2+
	TxCLK OUT-	33	11	CK1IN-
	TxCLK OUT+	32	12	CK1IN+
LVDS – National DS90CF561 (2nd data-Even chip)	TxOut0-	41	13	R2IN0-
	TxOut0+	40	14	R2IN0+
	TxOut1-	39	15	R2IN1-
	TxOut1+	38	16	R2IN1+
	TxOut2-	35	17	R2IN2-
	TxOut2+	34	18	R2IN2+
	TxCLK OUT-	33	19	CK2IN-
	TxCLK OUT+	32	20	CK2IN+
DK6555X connector J5 (50 pin)	Pin Name	Pin #		
	VDDSAFE	1	1&2	VDD (5V)
	GND	14,17 (any GND)	3&4	GND

From DK board to LVDS Transmitter

			DK6555X connector J5 (50 pin) & J11 (noted)	
	Pin #	Pin Name	Pin Name	Pin #
LVDS – National DS90CF561 (1st data- Odd chip)	44	TxIN0	P24	2 (J11)
	45	TxIN1	P25	4 (J11)
	47	TxIN2	P26	6 (J11)
	48	TxIN3	P27	8 (J11)
	1	TxIN4	P28	10 (J11)
	3	TxIN5	P29	12 (J11)
	4	TxIN6	P12	33
	6	TxIN7	P13	34
	7	TxIN8	P14	36
	9	TxIN9	P15	37
	10	TxIN10	P16	39
	12	TxIN11	P17	40
	13	TxIN12	P0	15
	15	TxIN13	P1	16
	16	TxIN14	P2	18
	18	TxIN15	P3	19
	19	TxIN16	P4	21
	20	TxIN17	P5	22
	22	TxIN18	LP	10
	23	TxIN19	FLM	11
	25	TxIN20	DE	8
	26	TxCLKIN	SHFCLK	13
	Pin #	Pin Name	Pin Name	Pin #
LVDS – National DS90CF561 (2nd data- Even chip)	44	TxIN0	P30	14 (J11)
	45	TxIN1	P31	16 (J11)
	47	TxIN2	P32	18 (J11)
	48	TxIN3	P33	20 (J11)
	1	TxIN4	P34	22(J11)
	3	TxIN5	P35	24 (J11)
	4	TxIN6	P18	42
	6	TxIN7	P19	43
	7	TxIN8	P20	45
	9	TxIN9	P21	46
	10	TxIN10	P22	49
	12	TxIN11	P23	24
	13	TxIN12	P6	25
	15	TxIN13	P7	27
	16	TxIN14	P8	28
	18	TxIN15	P9	30
	19	TxIN16	P10	31
	20	TxIN17	P11	10
	22	TxIN18	GND	6
	23	TxIN19	GND	9
	24	TxIN20	GND	12
	26	TxCLKIN	SHFCLK	13
Power and Ground pins for both LVDS Transmitter chips				
2,8,14,21,37,*29	Vcc, LVDS Vcc, *PLL Vcc		Vcc	4
5,11,17,24,46,42,3 6,31,*30,*28	GND, LVDS GND, *PLL GND		GND	20,23,26,29,32,35,38,41, 44,47,50

*PLL Vcc plane needs to be isolated, see LVDS datasheets for more information

Interfacing 6555x with a Samsung LT133X1-124

Panel General Description:

Resolution:	1024 x 768	Panel Voltage range:	3.3 volts (4v max.)
Type:	13.3" XGA TFT	Pixel/SHFCLK:	1
Pixel Depth:	6 bits/pixel	Interface:	18 single channel 3.3V LVDS

DK board to LVDS Transmitter

DK6555X connector J5 (50 pin)		LVDS – Texas Instruments SN75LVDS83	
Pin Name	Pin #	Pin #	Pin Name
P18	42	51	TxIN0
P19	43	52	TxIN1
P20	45	54	TxIN2
P21	46	55	TxIN3
P22	48	56	TxIN4
P23	49	3	TxIN6
P10	30	4	TxIN7
P11	31	6	TxIN8
P12	33	7	TxIN9
P13	34	11	TxIN12
P14	36	12	TxIN13
P15	37	14	TxIN14
P2	18	15	TxIN15
P3	19	19	TxIN18
P4	21	20	TxIN19
P5	22	22	TxIN20
P6	24	23	TxIN21
P7	25	24	TxIN22
LP	10	27	TxIN24
FLM	11	28	TxIN25
DE	8	30	TxIN26
SHFCLK	13	31	TxCLKIN
Vcc (3.3v)	4	1,9,26,44,*34	Vcc, LVDS Vcc, *PLL Vcc
Vcc(3.3v)	4	17,32	#CLKSEL, ®SHTDN
GND	20,23,26,29,32,35,38,41,44,47,50	05,13,21,29,*33,*35,36,43,49,53	GND, LVDS GND, *PLL GND

*PLL Vcc plane needs to be isolated, see LVDS datasheets for more information

#CLKSEL is pulled high to select rising edge of clock.

®Please see LVDS datasheet for more information

LVDS transmitter output to Panel 8 pin connector

LVDS – Texas Instrument SN75LVDS83		Samsung LT133X-124, 8 pin connector	
Pin Name	Pin #	Pin #	Pin Name
TxOut0-	48	5	R1IN0-
TxOut0+	47	6	R1IN0+
TxOut1-	46	8	R1IN1-
TxOut1+	45	9	R1IN1+
TxOut2-	42	11	R1IN2-
TxOut2+	41	12	R1IN2+
TxCLK OUT-	40	14	CK1IN-
TxCLK OUT+	39	15	CK1IN+
DK6555X connector J5 (50 pin)			
Pin Name	Pin #	17,18	No connect
VDDSAFE(3.3v)	1	1,2	VDD (5V)
GND	14,17 (any GND)	3,4,7,10,13,16,19,20	GND

Interfacing 6555x with a Hitachi TX34D61VC1CAD

Panel General Description:

Resolution:	1024 x 768	Panel Voltage range:	3.3 volts (4v max.)
Type:	13.3" XGA TFT	Pixel/SHFCLK:	1
Pixel Depth:	6 bits/pixel	Interface:	single channel 3.3V LVDS

DK board to LVDS Transmitter

DK6555X connector J5(50 pin)		LVDS – Texas Instruments SN75LVDS83	
Pin Name	Pin #	Pin #	Pin Name
P18	42	51	TxIN0
P19	43	52	TxIN1
P20	45	54	TxIN2
P21	46	55	TxIN3
P22	48	56	TxIN4
P23	49	3	TxIN6
P10	30	4	TxIN7
P11	31	6	TxIN8
P12	33	7	TxIN9
P13	34	11	TxIN12
P14	36	12	TxIN13
P15	37	14	TxIN14
P2	18	15	TxIN15
P3	19	19	TxIN18
P4	21	20	TxIN19
P5	22	22	TxIN20
P6	24	23	TxIN21
P7	25	24	TxIN22
LP	10	27	TxIN24
FLM	11	28	TxIN25
DE	8	30	TxIN26
SHFCLK	13	31	TxCLKIN
Vcc (3.3v)	4	1,9,26,44,*34	Vcc, LVDS Vcc, *PLL Vcc
Vcc(3.3v)	4	17,32	#CLKSEL, [Ⓢ] SHTDN
GND	20,23,26,29,32,35,38,41,44,47,50	05,13,21,29,*33,*35,36,43,49,53	GND, LVDS GND, *PLL GND

*PLL Vcc plane needs to be isolated, see LVDS datasheets for more information

#CLKSEL is pulled high to select rising edge of clock.

[Ⓢ]Please see LVDS datasheet for more information

LVDS transmitter output to Panel 21 pin connector*

LVDS – Texas Instrument SN75LVDS83		Hitachi TX34D61VC1CAD, 21 pin connector*	
Pin Name	Pin #	Pin #	Pin Name
TxOut0-	48	11	IN0-
TxOut0+	47	10	IN0+
TxOut1-	46	14	IN1-
TxOut1+	45	13	IN1+
TxOut2-	42	17	IN2-
TxOut2+	41	16	IN2+
TxCLK OUT-	40	8	CK IN-
TxCLK OUT+	39	7	CK IN+
DK6555X connector J5(50 pin)			
Pin Name	Pin #	1,2,3	No connect
VDDSAFE(3.3v)	1	4,5,6	VDD
GND	14,17 (any GND)	9,12,15,18,21	VSS

*JAE F1-WE21P-HF

Chapter 5

System Testing

Suggested ZV Port Manufacturing Test via the PCMCIA Socket

Hardware and Software Overview

Figure 5-1 shows a typical hardware and software structure for ZV Port testing. A simple hardware module specifically designed for ZV testing is connected to the PCMCIA/ZV port. This module generates a video test pattern which the HiQVideo™ device writes into the video capture buffer located in an off-screen area of the main display memory.

Standard Card Services and Socket Services software (not provided by CHIPS) can be used to put the PCMCIA Host Adapter into the ZV mode. A relatively simple test program (source code included in this application note) enables the video capture mode in the CHIPS HiQVideo™ device. Once the ZV mode is enabled in both the HiQVideo™ controller and PCMCIA Host Adapter, the video pattern supplied on the PCMCIA/ZV connector is written into the video capture buffer, where it can be checked to verify successful capture.

CHIPS has built and tested a stripped down version of this structure that uses only the video capture port of the HiQVideo™ controller, without a PCMCIA/ZV Host Adapter or PCMCIA/ZV connector. This application note includes a schematic diagram of the video test pattern generator, and also the GAL equations and source code for the test program. CHIPS has not as yet attempted to test with a PCMCIA/ZV Host Adapter or Card/Socket Services software to determine what additional test instructions, if any, may be needed to put the PCMCIA/ZV Host Adapter into ZV mode. The video pattern generator that has been used so far does not mimic the full responses of a true PCMCIA card. So additional work may be needed in the test program to properly communicate with Card and Socket Services in the absence of an actual PCMCIA card.

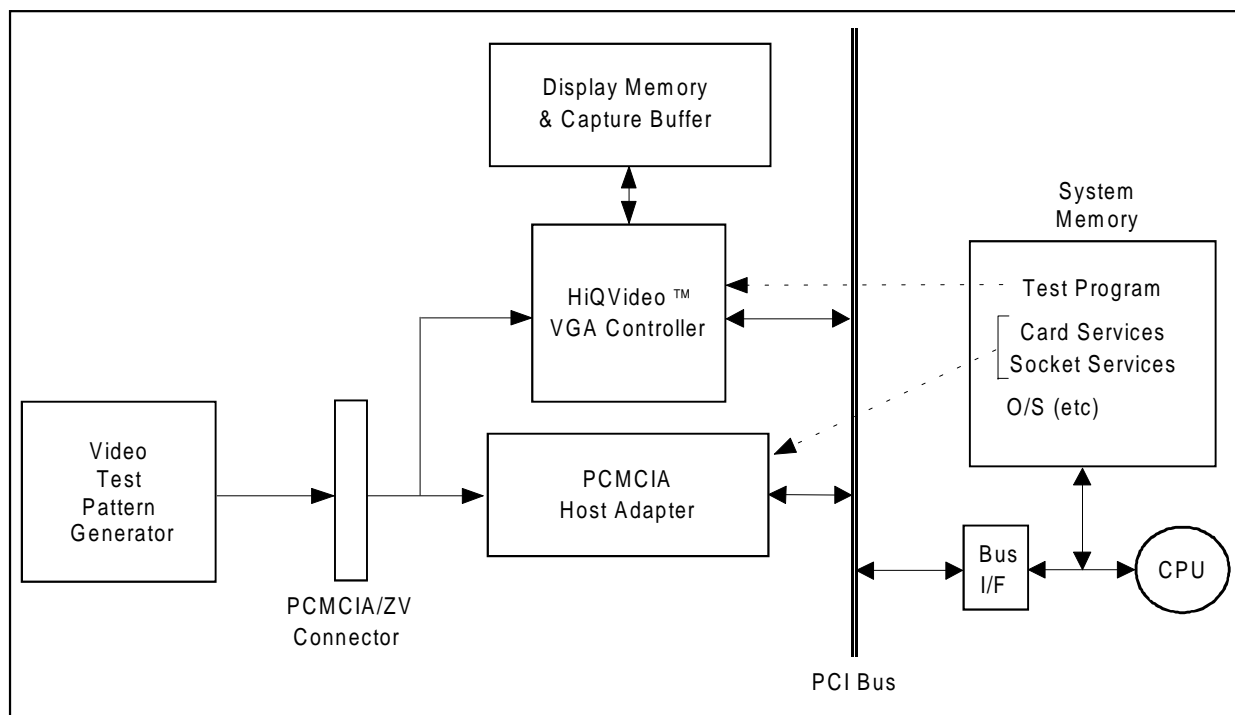


Figure 5-1: Hardware and Software for ZV Test

Video Test Pattern Generator

Figure 5-2 shows a schematic for the video test pattern generator that CHIPS has actually tested. An LM555 timer circuit generates a 1 MHz reference clock, which is divided by a 7-bit counter in a GAL22V10 to produce a simulated HSYNC. A second GAL22V10 divides HSYNC again to produce a simulated VSYNC.

Because of component tolerances, the 1 MHz reference frequency may actually be anywhere from about 500 KHz to 1 MHz. The exact frequency isn't critical, as long as GAL22V10 speed limitations are satisfied.

The 16-bit data pattern is AAAAh or 5555h when the LSB of the HSYNC counter is zero or one, respectively.

The hardware jumper, W1, can be used to disable video pattern generation during system initialization. The ZV signals are tri-stated when disabled so they will not conflict with PCMCIA Host Adapter output signals before the PCMCIA controller has been put into ZV mode. For a more automated testing environment, a GPIO pin from the HiQVideo™ controller or other source could be used instead of a manual jumper to start and stop the test pattern under software control.

A 40-pin "header" provides the connector for a ribbon cable to a corresponding connector on the CHIPS DK65550 evaluation board. A separate 12-pin connector provides +5V power for the video test pattern generator.

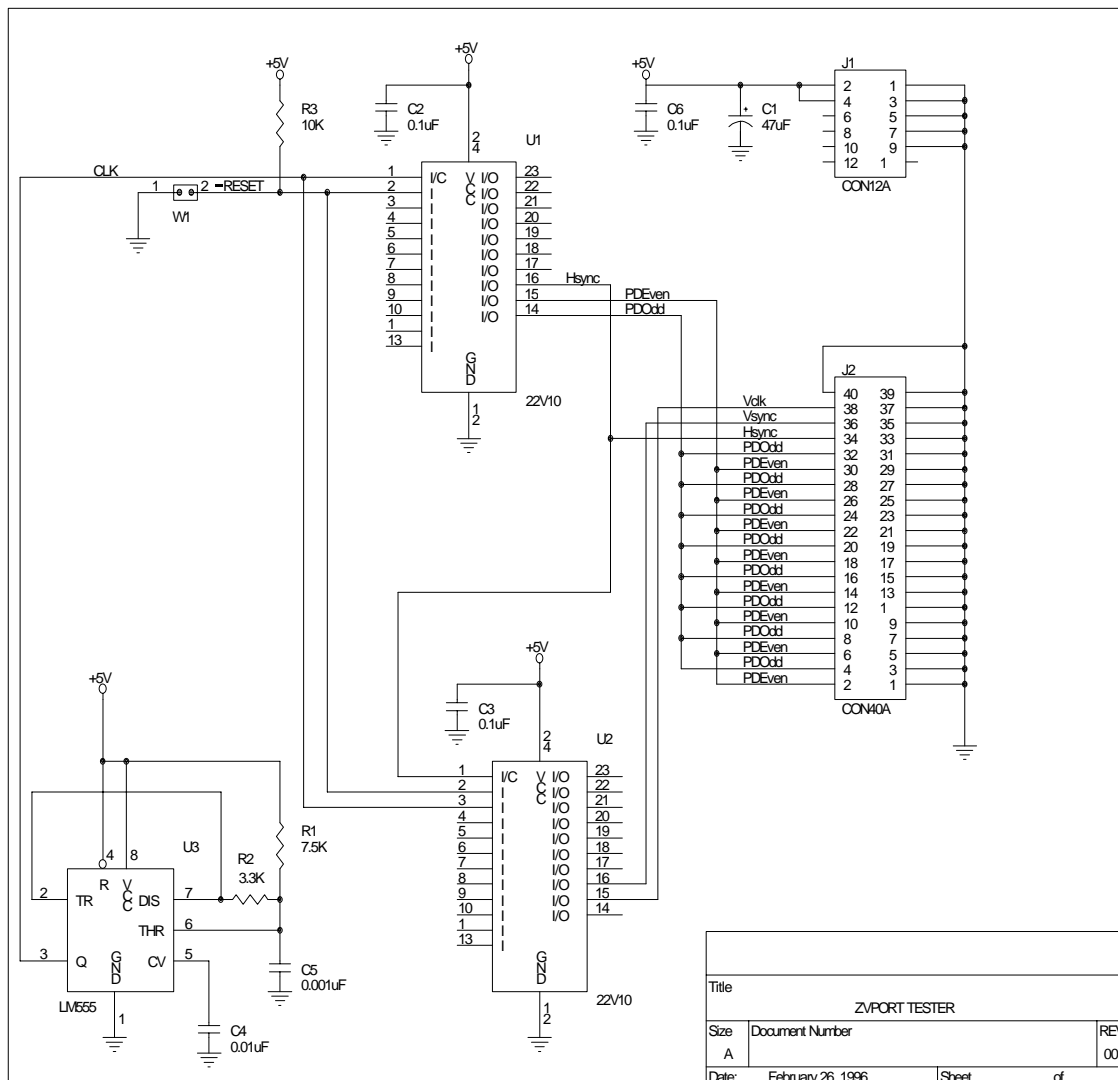


Figure 5-2: Schematic for the Video Test Pattern Generator

Timing Diagrams

Figures 5-3 and 5-4 below show the timing diagrams for the video test pattern generator. The HSYNC counter divides the 1 MHz reference clock by 96 (60h) to generate HSYNC and the AAAAh/5555h data selection signals. The count sequence is 0 through 5Fh. HSYNC is high during counts 20h through 5Fh, low during counts 0 through 1Fh. The frequency of the data pixels is 1 MHz, and the frequency of HSYNC is 10.4 KHz. (For board-level manufacturing test purposes, exact NTSC frequencies and resolutions are not needed.) A total of 96 pixels are generated during each cycle of HSYNC.

In PCMCIA/ZV terminology, HSYNC is actually referred to as HREF. The high state of HREF corresponds to the “active display” interval, and the low state corresponds to horizontal blanking.

The VSYNC counter divides HSYNC by 36 (24h) to generate VSYNC. The count sequence is 0 through 23h. VSYNC is high during counts 20h through 23h.

The VCLK output from the VSYNC GAL is just a buffered, non-inverted version of the CLK input. VCLK is tri-stated when –RESET is low. Unless –RESET is synchronized to CLK, the initial cycle of VCLK following –RESET may be shortened. This should not be a problem, since the video pattern is free running, and capture actually starts when the HiQVideo(is enabled for video capture (ZV mode).

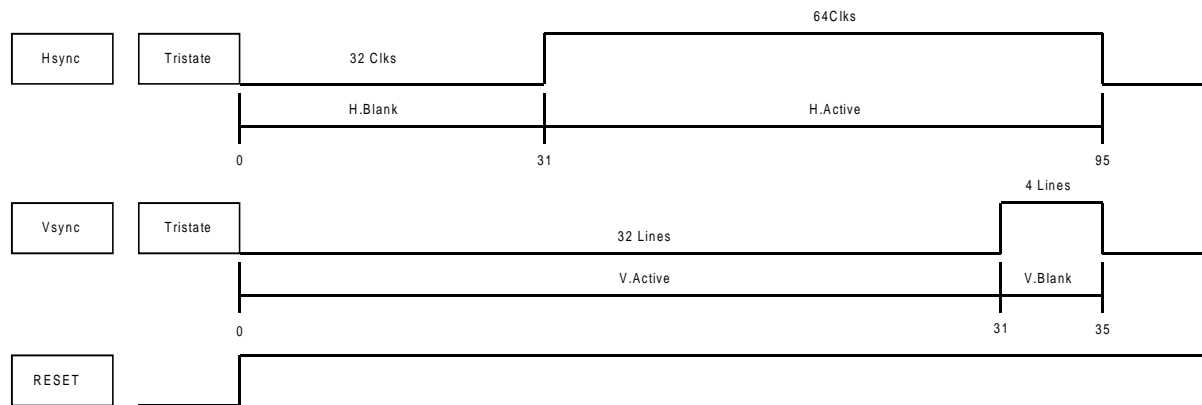


Figure 5-3: Hsync and Vsync Timing

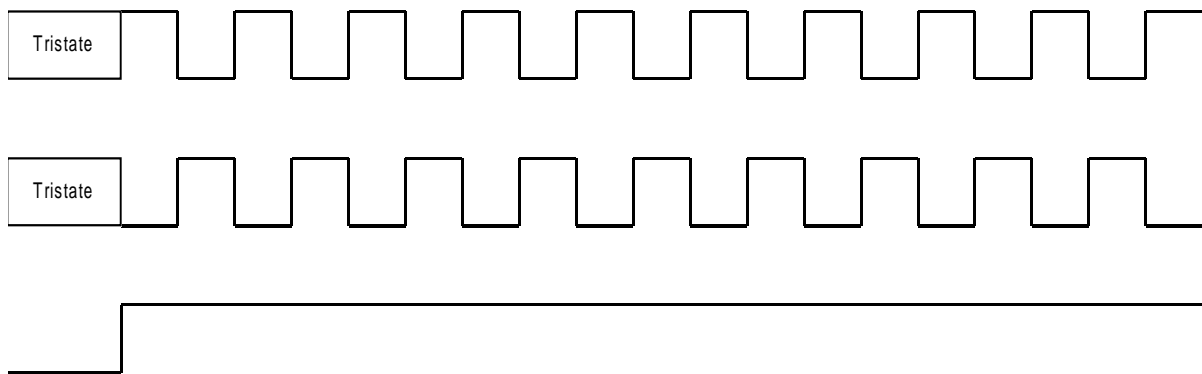


Figure 5-4: Data Enable Timing

Equations for HSYNC GAL

```

*****
*
*                                     ZVPORT1.P
*****
*

CUPL          3.2a Serial# MD-32A-6582
Device        g22v10 Library DLIB-h-25-1
Created       Wed Apr 17 17:09:39 1996
Name          ZVPORT1.PLD
Partno        None
Revision      00
Date          2-15-96
Designer      POW
Company       CHIPS AND TECHNOLOGIES
Assembly      None
Location      None

=====
=
Expanded Product Terms
=====
=

Hsync =>
    Q5
    # Q6

Hsync.oe =>
    !RESET

PDEven =>
    Q0

PDEven.oe =>
    !RESET

PDOdd =>
    !Q0

PDOdd.oe =>
    !RESET

Q0.ar =>
    RESET

Q0.d =>
    !Q0 & Q5 & !Q6
    # !Q0 & !Q5

Q0.sp =>
    0

```

Equations for HSYNC GAL (continued)

Q1.ar =>
RESET

Q1.d =>
!Q0 & Q1 & Q5 & !Q6
Q0 & !Q1 & Q5 & !Q6
!Q0 & Q1 & !Q5
Q0 & !Q1 & !Q5

Q1.sp =>
0

Q2.ar =>
RESET

Q2.d =>
!Q0 & Q1 & Q2 & Q5 & !Q6
!Q1 & Q2 & Q5 & !Q6
Q0 & Q1 & !Q2 & Q5 & !Q6
!Q0 & Q1 & Q2 & !Q5
!Q1 & Q2 & !Q5
Q0 & Q1 & !Q2 & !Q5

Q2.sp =>
0

Q3.ar =>
RESET

Q3.d =>
!Q0 & Q1 & Q2 & Q3 & Q5 & !Q6
Q0 & Q1 & Q2 & !Q3 & !Q5
Q1 & !Q2 & Q3 & Q5 & !Q6
!Q2 & Q3 & !Q5
!Q1 & Q3 & Q5 & !Q6
!Q0 & Q1 & Q2 & Q3 & !Q5
Q0 & Q1 & Q2 & !Q3 & Q5 & !Q6
!Q1 & Q2 & Q3 & !Q5

Q3.sp =>
0

Equations for HSYNC GAL (continued)

Q4.ar =>
RESET

Q4.d =>
 !Q0 & Q1 & Q2 & Q3 & Q4 & !Q5 & Q6
 # Q0 & Q1 & Q2 & Q3 & !Q4 & !Q6
 # Q0 & Q1 & Q2 & Q3 & !Q4 & !Q5 & Q6
 # !Q3 & Q4 & !Q5
 # Q1 & Q2 & !Q3 & Q4 & Q5 & !Q6
 # Q1 & !Q2 & Q4 & Q5 & !Q6
 # !Q1 & Q4 & Q5 & !Q6
 # !Q2 & Q3 & Q4 & !Q5
 # !Q1 & Q2 & Q3 & Q4 & !Q5
 # !Q0 & Q1 & Q2 & Q3 & Q4 & !Q6

Q4.sp =>
0

Q5.ar =>
RESET

Q5.d =>
 !Q0 & Q1 & Q2 & Q3 & Q4 & Q5 & !Q6
 # Q0 & Q1 & Q2 & Q3 & Q4 & !Q5 & !Q6
 # Q1 & Q2 & Q3 & !Q4 & Q5 & !Q6
 # !Q3 & Q5 & !Q6
 # Q1 & !Q2 & Q3 & Q5 & !Q6
 # !Q1 & Q3 & Q5 & !Q6

Q5.sp =>
0

Equations for HSYNC GAL (continued)

```
Q6.ar =>  
    RESET
```

```
Q6.d  =>  
    !Q0 & Q1 & Q2 & Q3 & Q4 & !Q5 & Q6  
    # Q0 & Q1 & Q2 & Q3 & Q4 & Q5 & !Q6  
    # Q1 & Q2 & Q3 & !Q4 & !Q5 & Q6  
    # !Q3 & !Q5 & Q6  
    # Q1 & !Q2 & Q3 & !Q5 & Q6  
    # !Q1 & Q3 & !Q5 & Q6
```

```
Q6.sp =>  
    0
```

```
state =>  
    Q0 , Q1 , Q2 , Q3 , Q4 , Q5 , Q6
```

```
Q0.oe =>  
    1
```

```
Q1.oe =>  
    1
```

```
Q2.oe =>  
    1
```

```
Q3.oe =>  
    1
```

```
Q4.oe =>  
    1
```

```
Q5.oe =>  
    1
```

```
Q6.oe =>  
    1
```

Equations for HSYNC GAL (continued)

=====						
=						
Symbol Table						
=====						
=						
Pin Pol	Variable Name	Ext	Pin	Type	Pterms Used	Max Pterms Min Level
----	-----	---	---	----	-----	-----
	CLK		1	V	-	-
	Hsync		16	V	2	12
	Hsync	oe	16	X	1	1
	PDEven		15	V	1	10
	PDEven	oe	15	X	1	1
	PDOdd		14	V	1	8
	PDOdd	oe	14	X	1	1
	Q0		23	V	-	-
	Q0	ar	23	X	1	1
	Q0	d	23	X	2	8
	Q0	sp	23	X	1	1
	Q1		22	V	-	-
	Q1	ar	22	X	1	1
	Q1	d	22	X	4	10
	Q1	sp	22	X	1	1
	Q2		21	V	-	-
	Q2	ar	21	X	1	1
	Q2	d	21	X	6	12
	Q2	sp	21	X	1	1
	Q3		20	V	-	-
	Q3	ar	20	X	1	1
	Q3	d	20	X	8	14
	Q3	sp	20	X	1	1
	Q4		19	V	-	-
	Q4	ar	19	X	1	1
	Q4	d	19	X	10	16
	Q4	sp	19	X	1	1
	Q5		18	V	-	-
	Q5	ar	18	X	1	1
	Q5	d	18	X	6	16
	Q5	sp	18	X	1	1
	Q6		17	V	-	-
	Q6	ar	17	X	1	1
	Q6	d	17	X	6	14
	Q6	sp	17	X	1	1
!	RESET		2	V	-	-
	state		0	F	-	-
	Q0	oe	23	D	1	1
	Q1	oe	22	D	1	1
	Q2	oe	21	D	1	1
	Q3	oe	20	D	1	1
	Q4	oe	19	D	1	1
	Q5	oe	18	D	1	1
	Q6	oe	17	D	1	1

Equations for HSYNC GAL (continued)

LEGEND	F : field	D : default variable	M : extended node
	N : node	I : intermediate variable	T : function
	V : variable	X : extended variable	U : undefined

```
=====
=
```

Fuse Plot

```
=====
=
```

SP

```
05764 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

AR

```
00000 ----x-----
```

Pin #23 05808 Mode -x

```
00044 -----
00088 --x-----x--x-----
00132 --x-----x-----
00176 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00220 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00264 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00308 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00352 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00396 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

Pin #22 05810 Mode -x

```
00440 -----
00484 --x---x-----x--x-----
00528 ---x--x-----x--x-----
00572 --x---x-----x-----
00616 ---x--x-----x-----
00660 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00704 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00748 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00792 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00836 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00880 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

Pin #21 05812 Mode -x

```
00924 -----
00968 --x---x---x-----x--x-----
01012 -----x---x-----x--x-----
01056 ---x--x--x-----x--x-----
01100 --x---x---x-----x-----
01144 -----x---x-----x-----
01188 ---x--x--x-----x-----
01232 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01276 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01320 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01364 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01408 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01452 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```


Equations for HSYNC GAL (continued)

Pin #20 05814 Mode -x

```

01496 -----
01540 --x---x---x---x-----x--x-----
01584 ---x---x---x---x-----x-----
01628 -----x--x---x-----x--x-----
01672 -----x---x---x-----x-----
01716 -----x-----x-----x--x-----
01760 --x---x---x---x-----x-----
01804 ---x---x---x---x-----x--x-----
01848 -----x---x---x-----x-----
01892 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01936 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01980 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02024 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02068 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02112 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

```

Pin #19 05816 Mode -x

```

02156 -----
02200 --x---x---x---x---x---x---x-----
02244 ---x---x---x---x---x-----x-----
02288 ---x---x---x---x---x---x---x-----
02332 -----x---x---x-----x-----
02376 -----x---x---x---x---x---x-----
02420 -----x--x-----x---x---x-----
02464 -----x-----x---x---x-----
02508 -----x---x---x---x-----
02552 -----x---x---x---x---x-----
02596 --x---x---x---x---x-----x-----
02640 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02684 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02728 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02772 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02816 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02860 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

```

Equations for HSYNC GAL (continued)

```

Pin #18 05818 Mode -x
02904 -----
02948 --x---x---x---x---x---x---x-----
02992 ---x---x---x---x---x---x---x-----
03036 -----x---x---x---x---x---x-----
03080 -----x-----x---x-----
03124 -----x---x---x-----x---x-----
03168 -----x-----x-----x---x-----
03212 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03256 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03300 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03344 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03388 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03432 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03476 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03520 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03564 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03608 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #17 05820 Mode -x
03652 -----
03696 --x---x---x---x---x---x---x-----
03740 ---x---x---x---x---x---x---x-----
03784 -----x---x---x---x---x---x-----
03828 -----x-----x---x-----
03872 -----x---x---x---x---x---x-----
03916 -----x-----x---x---x-----
03960 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04004 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04048 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04092 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04136 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04180 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04224 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04268 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #16 05822 Mode --
04312 ----x-----
04356 -----x-----
04400 -----x-----
04444 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04488 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04532 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04576 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04620 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04664 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04708 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04752 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04796 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04840 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

```

Equations for HSYNC GAL (continued)

```

Pin #15  05824 Mode  --
04884  ----x-----
04928  ---x-----
04972  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05016  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05060  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05104  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05148  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05192  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05236  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05280  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05324  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #14  05826 Mode  --
05368  ----x-----
05412  ---x-----
05456  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05500  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05544  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05588  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05632  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05676  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05720  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

```

LEGEND X : fuse not blown
 - : fuse blown

Equations for HSYNC GAL (continued)

=====

=

Chip Diagram

=====

=

		ZVPORT1.P			
CLK	x---	1	24	---x	Vcc
!RESET	x---	2	23	---x	Q0
	x---	3	22	---x	Q1
	x---	4	21	---x	Q2
	x---	5	20	---x	Q3
	x---	6	19	---x	Q4
	x---	7	18	---x	Q5
	x---	8	17	---x	Q6
	x---	9	16	---x	Hsync
	x---	10	15	---x	PDEven
	x---	11	14	---x	PDOdd
GND	x---	12	13	---x	

Equations for VSYNC GAL

```
*****
*
```

ZVPORT2.P

```
*****
*
```

```
CUPL          3.2a Serial# MD-32A-6582
Device        g22v10 Library DLIB-h-25-1
Created       Wed Apr 17 17:09:31 1996
Name          ZVPORT2.PLD
Partno        None
Revision      00
Date          2-15-96
Designer      POW
Company       CHIPS AND TECHNOLOGIES
Assembly      None
Location      None
```

```
=====
=
```

Expanded Product Terms

```
=====
=
```

```
Q0.ar =>
  RESET
```

```
Q0.d  =>
  !Q0 & !Q2 & !Q3 & !Q4 & Q5
  # !Q0 & !Q5
```

```
Q0.sp =>
  0
```

```
Q1.ar =>
  RESET
```

```
Q1.d  =>
  !Q0 & Q1 & !Q2 & !Q3 & !Q4 & Q5
  # Q0 & !Q1 & !Q2 & !Q3 & !Q4 & Q5
  # !Q0 & Q1 & !Q5
  # Q0 & !Q1 & !Q5
```

```
Q1.sp =>
  0
```

Equations for VSYNC GAL (continued)

```
Q2.ar =>  
  RESET
```

```
Q2.d =>  
  !Q0 & Q1 & Q2 & !Q5  
  # Q0 & Q1 & !Q2 & !Q5  
  # !Q1 & Q2 & !Q5
```

```
Q2.sp =>  
  0
```

```
Q3.ar =>  
  RESET
```

```
Q3.d =>  
  !Q0 & Q1 & Q2 & Q3 & !Q5  
  # Q0 & Q1 & Q2 & !Q3 & !Q5  
  # !Q1 & Q2 & Q3 & !Q5  
  # !Q2 & Q3 & !Q5
```

```
Q3.sp =>  
  0
```

```
Q4.ar =>  
  RESET
```

```
Q4.d =>  
  !Q0 & Q1 & Q2 & Q3 & Q4 & !Q5  
  # Q0 & Q1 & Q2 & Q3 & !Q4 & !Q5  
  # Q1 & Q2 & !Q3 & Q4 & !Q5  
  # !Q2 & Q4 & !Q5  
  # !Q1 & Q2 & Q4 & !Q5
```

```
Q4.sp =>  
  0
```

```
Q5.ar =>  
  RESET
```

```
Q5.d =>  
  !Q0 & Q1 & !Q2 & !Q3 & !Q4 & Q5  
  # Q0 & Q1 & Q2 & Q3 & Q4 & !Q5  
  # !Q1 & !Q2 & !Q3 & !Q4 & Q5
```

```
Q5.sp =>  
  0
```

Equations for VSYNC GAL (continued)

```
Q6 =>  
    RESET
```

```
Q6 =>  
    0
```

```
Vclk =>  
    CLK
```

```
Vclk.oe =>  
    !RESET
```

```
Vsync =>  
    Q5
```

```
Vsync.oe =>  
    !RESET
```

```
state =>  
    Q0 , Q1 , Q2 , Q3 , Q4 , Q5
```

```
Q0.oe =>  
    1
```

```
Q1.oe =>  
    1
```

```
Q2.oe =>  
    1
```

```
Q3.oe =>  
    1
```

```
Q4.oe =>  
    1
```

```
Q5.oe =>  
    1
```

Equations for VSYNC GAL (continued)

=====

=

Symbol Table

=====

=

Pin Pol	Variable Name	Ext	Pin	Type	Pterms Used	Max Pterms	Min Level
---	-----	---	---	----	-----	-----	-----
	CLK		3	V	-	-	-
	Hsync		1	V	-	-	-
	Q0		23	V	-	-	-
	Q0	ar	23	X	1	1	1
	Q0	d	23	X	2	8	1
	Q0	sp	23	X	1	1	1
	Q1		22	V	-	-	-
	Q1	ar	22	X	1	1	1
	Q1	d	22	X	4	10	1
	Q1	sp	22	X	1	1	1
	Q2		21	V	-	-	-
	Q2	ar	21	X	1	1	1
	Q2	d	21	X	3	12	1
	Q2	sp	21	X	1	1	1
	Q3		20	V	-	-	-
	Q3	ar	20	X	1	1	1
	Q3	d	20	X	4	14	1
	Q3	sp	20	X	1	1	1
	Q4		19	V	-	-	-
	Q4	ar	19	X	1	1	1
	Q4	d	19	X	5	16	1
	Q4	sp	19	X	1	1	1
	Q5		18	V	-	-	-
	Q5	ar	18	X	1	1	1
	Q5	d	18	X	3	16	1
	Q5	sp	18	X	1	1	1
	Q6	ar	0	I	1	-	-
	Q6	sp	0	I	1	-	-
!	RESET		2	V	-	-	-
	Vclk		15	V	1	10	1
	Vclk	oe	15	X	1	1	1
	Vsync		16	V	1	12	1
	Vsync	oe	16	X	1	1	1
	state		0	F	-	-	-
	Q0	oe	23	D	1	1	0
	Q1	oe	22	D	1	1	0
	Q2	oe	21	D	1	1	0
	Q3	oe	20	D	1	1	0
	Q4	oe	19	D	1	1	0
	Q5	oe	18	D	1	1	0

Equations for VSYNC GAL (continued)

LEGEND	F : field	D : default variable	M : extended node
	N : node	I : intermediate variable	T : function
	V : variable	X : extended variable	U : undefined

```
=====
=
```

Fuse Plot

```
=====
=
```

SP

```
05764 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

AR

```
00000 ----x-----
```

Pin #23 05808 Mode -x

```
00044 -----
```

```
00088 --x-----x--x--x--x--x-----
```

```
00132 --x-----x-----
```

```
00176 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

```
00220 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

```
00264 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

```
00308 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

```
00352 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

```
00396 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

Pin #22 05810 Mode -x

```
00440 -----
```

```
00484 --x---x--x--x--x--x-----
```

```
00528 ---x--x--x--x--x--x-----
```

```
00572 --x---x-----x-----
```

```
00616 ---x-x-----x-----
```

```
00660 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

```
00704 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

```
00748 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

```
00792 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

```
00836 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

```
00880 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

Pin #21 05812 Mode -x

```
00924 -----
```

```
00968 --x---x--x-----x-----
```

```
01012 ---x--x--x-----x-----
```

```
01056 -----x---x-----x-----
```

```
01100 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

```
01144 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

```
01188 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

```
01232 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

```
01276 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

```
01320 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

```
01364 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

```
01408 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

```
01452 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

Equations for VSYNC GAL (continued)

Pin #20 05814 Mode -x

```
01496 -----
01540 --x---x---x---x-----x-----
01584 ---x---x---x---x-----x-----
01628 -----x---x---x-----x-----
01672 -----x---x-----x-----
01716 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01760 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01804 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01848 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01892 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01936 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
01980 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02024 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02068 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02112 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

Pin #19 05816 Mode -x

```
02156 -----
02200 --x---x---x---x---x---x-----
02244 ---x---x---x---x---x---x-----
02288 -----x---x---x---x---x-----
02332 -----x-----x---x-----
02376 -----x---x-----x---x-----
02420 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02464 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02508 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02552 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02596 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02640 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02684 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02728 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02772 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02816 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
02860 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

Equations for VSYNC GAL (continued)

Pin #18 05818 Mode -x

```
02904 -----
02948 --x---x--x---x---x---x-----
02992 ---x---x---x---x---x---x-----
03036 -----x---x---x---x---x-----
03080 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03124 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03168 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03212 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03256 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03300 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03344 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03388 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03432 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03476 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03520 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03564 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03608 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

Pin #17 05820 Mode xx

```
03652 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03696 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03740 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03784 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03828 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03872 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03916 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
03960 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04004 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04048 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04092 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04136 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04180 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04224 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04268 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

Pin #16 05822 Mode --

```
04312 ----x-----
04356 -----x-----
04400 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04444 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04488 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04532 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04576 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04620 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04664 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04708 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04752 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04796 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
04840 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

Equations for VSYNC GAL (continued)

```

Pin #15  05824 Mode  --
04884  ----x-----
04928  -----x-----
04972  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05016  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05060  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05104  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05148  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05192  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05236  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05280  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05324  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #14  05826 Mode  xx
05368  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05412  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05456  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05500  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05544  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05588  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05632  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05676  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
05720  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

```

LEGEND X : fuse not blown
 - : fuse blown

```

=====
=
                                Chip Diagram
=====
=

```

ZVPORT2.P					
Hsync	x---	1	24	---x	Vcc
!RESET	x---	2	23	---x	Q0
CLK	x---	3	22	---x	Q1
	x---	4	21	---x	Q2
	x---	5	20	---x	Q3
	x---	6	19	---x	Q4
	x---	7	18	---x	Q5
	x---	8	17	---	
	x---	9	16	---x	Vsync
	x---	10	15	---x	Vclk
	x---	11	14	---	
GND	x---	12	13	---	

Test Program for HiQVideo Setup & Verification

The test program initializes the HiQVideo(controller, waits for the video test pattern to be captured, and verifies the first two data words captured in the video capture buffer. A pass/fail result is displayed on the screen. The program is written in "C" (with various C++ style comments).

```

/
*****
*
* ZVTEST.C - Main module for a utility which performs memory testing on ZVPORT
*           for CHIPS' video products.
*
* Copyright (C) Chips and Technologies, Inc. Feb 23, 1996      Rev 1.2
* 1.0 --> 1.1 Revised 4/17/96 added 2nd single capture + some comments and changed to
Rev 1.1
* 1.1 --> 1.2 Revised 5/28/96 correct setting ZV Style connector XR60 from 00 to 03,
changed Rev to 1.2
*****
*****/

#include <conio.h>
#include <graph.h>
#include <stdio.h>
#include <dos.h>
#include <stdlib.h>
#include <time.h>

union   REGS    preg;           // register structure for int86

void setreg(int index, int offset, int value);
void sleep( clock_t wait );

void main( void )
{
    int SR01,XR0A,GR06,XRD0,XR60;
    unsigned int word1,word2;
    long n=0;

    /* Set to graphics MODE 03h */
    preg.h.ah= 0x00;
    preg.h.al= 0x03;
    int86(0x10,&preg,&preg);

    // Save XR0A, GR06, XR0E.
    outp(0x3d6,0x0a);
    XR0A=inp(0x3d7);

    outp(0x3d6,0x0a);
    outp(0x3d7,0x05); //Set XR0A for packed paged addressing so can read from
A000:000.
    outp(0x3ce,0x06);
    GR06=inp(0x3cf); //Save GR06

    outp(0x3ce,0x06);
    outp(0x3cf,0x04); //Set GR06 Memory Map Mode for A0000h-AFFFFh.
    outp(0x3d6,0x0e);
    outp(0x3d7,0x04); //Set XR0E to 4.

```

Test Program for HiQVideo Setup & Verification (continued)

```

    outp(0x3d6,0x60);
    XR60=inp(0x3d7); //Save XR60;
    outp(0x3d6,0xd0);
    XRD0=inp(0x3d7); //Save XRD0

    //clear memory to all 0s.
    _asm
    {
        push    bx
        push    ax
        push    cx
        push    es
        mov     ax,0a000h
        mov     es,ax
        mov     cx,07fffh
        mov     bx,0000h
        mov     ax,0000h

    L1:
        mov     es:[bx],ax
        add     bx,2
        loop    L1
        pop     es
        pop     cx
        pop     ax
        pop     bx
    }

    //      Set Registers for Capture.

    setreg(0x3d2,0x02,0x01); //Set MR02 to 01H (Non-Interlaced).
    setreg(0x3d2,0x04,0x00); //Set MR04 to 00H.
    setreg(0x3d2,0x06,0x00);
    setreg(0x3d2,0x07,0x00);
    setreg(0x3d2,0x08,0x04); //Set to second 256K of memory.
    setreg(0x3d2,0x0c,0x07); //Set Memory Width = 1 line = Pixel Width/4 -1 = 32/4-1=7.
    setreg(0x3d2,0x0e,0x00);
    setreg(0x3d2,0x10,0x1f); //Set Window to Pixel width so no cropping = 32 = 20H.
    setreg(0x3d2,0x11,0x00);
    setreg(0x3d2,0x12,0x00); //Set Window top = 00H.
    setreg(0x3d2,0x13,0x00);
    setreg(0x3d2,0x14,0x01); //Set Window bottom = 2 lines.
    setreg(0x3d2,0x15,0x00);
    setreg(0x3d6,0x60,0x03); //Set for ZV style Connector.
    setreg(0x3d6,0xd0,0x6F); //Set Multimedia enable & VAFC/Multimedia input Pins En-
able

    // Save SR01
    outp(0x3c4,0x01);
    SR01=inp(0x03c5);

    SR01=SR01|0x20;
    setreg(0x3c4,0x01,SR01); //Turn off screen

```

Test Program for HiQVideo Setup & Verification (continued)

```

    setreg(0x3d2,0x03,0x03);
                                //Set MR03 to 03H (1st Single capture ,Start Grab).
    sleep( (clock_t)3 * CLOCKS_PER_SEC );
                                //do nothing for 3 seconds to insure grab.
    setreg(0x3d2,0x03,0x03);
                                //Set MR03 to 03H (2nd Single capture ,Start Grab add-
ed                                4/17/96).
    sleep( (clock_t)3 * CLOCKS_PER_SEC );
                                //do nothing for 3 seconds to insure grab added 4/17/
96).

                                // Save the first two words in the capture buffer
_asm
{
    push    bx
    push    ax
    push    es
    mov     ax,0a000h
    mov     es,ax
    mov     cx,07ffffh
    mov     bx,0000h
    mov     ax,es:[bx]
    mov     word1,ax
    mov     ax,es:[bx+2]
    mov     word2,ax
    pop     es
    pop     ax
    pop     bx
}
SR01=SR01&0xdf;
setreg(0x3c4,0x01,SR01);

//Turn screen back on
//Restore registers.
setreg(0x3ce,0x06,GR06);
setreg(0x3d6,0x0a,XR0A);
setreg(0x3d6,0x0e,0x00);
setreg(0x3d6,0xd0,XRD0);
setreg(0x3d6,0x60,XR60);
setreg(0x3d2,0x03,0x00);

//Reset to mode 3+
preg.h.ah= 0x00;
preg.h.al= 0x03;
int86(0x10,&preg,&preg);

if(word1==0xaaaa && word2==0x5555) printf("ZVPORT TEST (REV 1.2)  PASSED\n");
if(word1!=0xaaaa) printf("ZVPORT TEST (REV 1.2) FAILED  READ %x instead of
AAAA\n",word1);
if(word2!=0x5555) printf("ZVPORT TEST (REV 1.2) FAILED  READ %x instead of
5555\n",word2);
}

```

Test Program for HiQVideo Setup & Verification (continued)

```
void setreg(int index,int offset,int value)
{
    // Write a specified value to an indexed register
    outp(index,offset);//Set index to offset.
    outp(index+1,value);//Set offset to value.
}

void sleep( clock_t wait )
{
    // Delay for specified number of seconds
    clock_t goal;
    goal = wait + clock();
    while( goal > clock() )
        ;
}
```


Enhancements to the Test Pattern Generator

Figure 5-5 shows an example of an untested schematic for a more enhanced video pattern generator. This example uses two EPROMs to generate the data pixels, based on the low-order four bits of the HSYNC and VSYNC counters. The VEN and HBLANK signals allow the data pattern to be shut off during horizontal blanking instead of continuing to run. An arbitrary data pattern can be placed into the EPROMs.

Both the enhanced video pattern generator and the original (non-EPROM) design work only in non-interlaced modes. They do not simulate an interlaced video pattern. This should be sufficient for board-level manufacturing tests since they test the solder connections on the board, not the HiQVideo™ silicon. The HiQVideo(controller is assumed to have already been tested at the chip level and possibly again during an incoming inspection process, and should not need in-circuit functional testing prior to final system test.

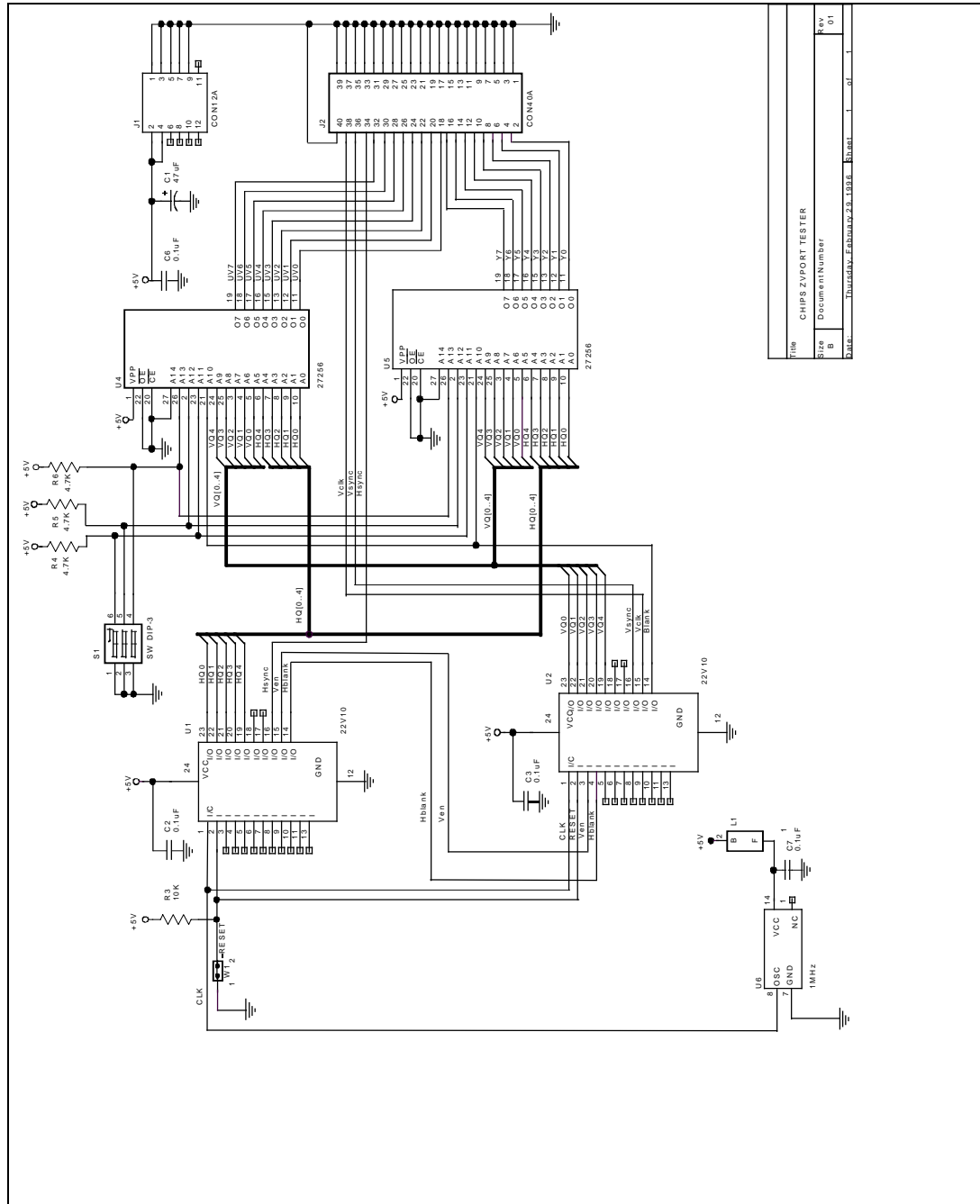


Figure 5-5: Enhanced Video Pattern Generator



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