2 Architecture Overview

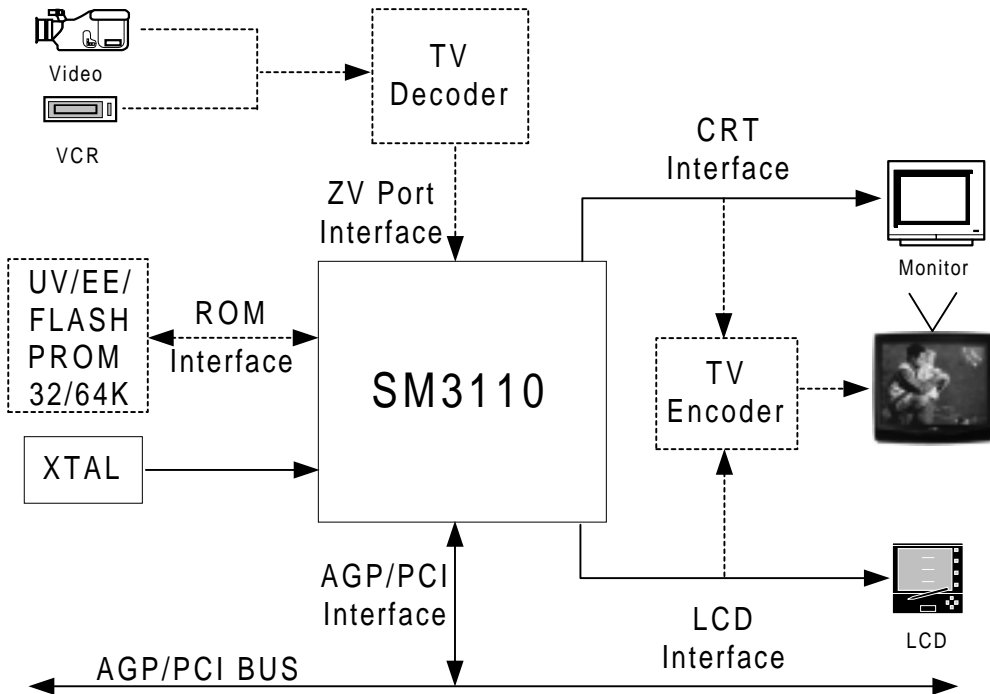# 2.1   System Configuration

Figure 2-1. Typical SM3110 System Configuration

The SM3110 is an integrated graphics accelerator designed for high performance in a limited space environment, such as a laptop computer. The SM3110 Graphics Accelerator has a number of interfaces to accommodate a variety of configurations and devices.

The host interface is glueless for a direct connection to either AGP or PCI buses. A Zoom Video input port (ZV Port) is provided to accept live video. A single external crystal supplies reference clock timing to three internal independently programmable Phase Locked Loops (PLL). The BIOS ROM port can access a separate graphics ROM or it can be converted for output to a digital TV encoder if the graphics ROM is not used in the system. The display outputs can drive a DSTN or TFT panel and a CRT monitor simultaneously. The data on two displays can be either the same or different, providing a flexible system configuration. Either display port can connect to a TV encoder for TV display. The DAC and clock synthesizers are also built in to minimize the need for external components.
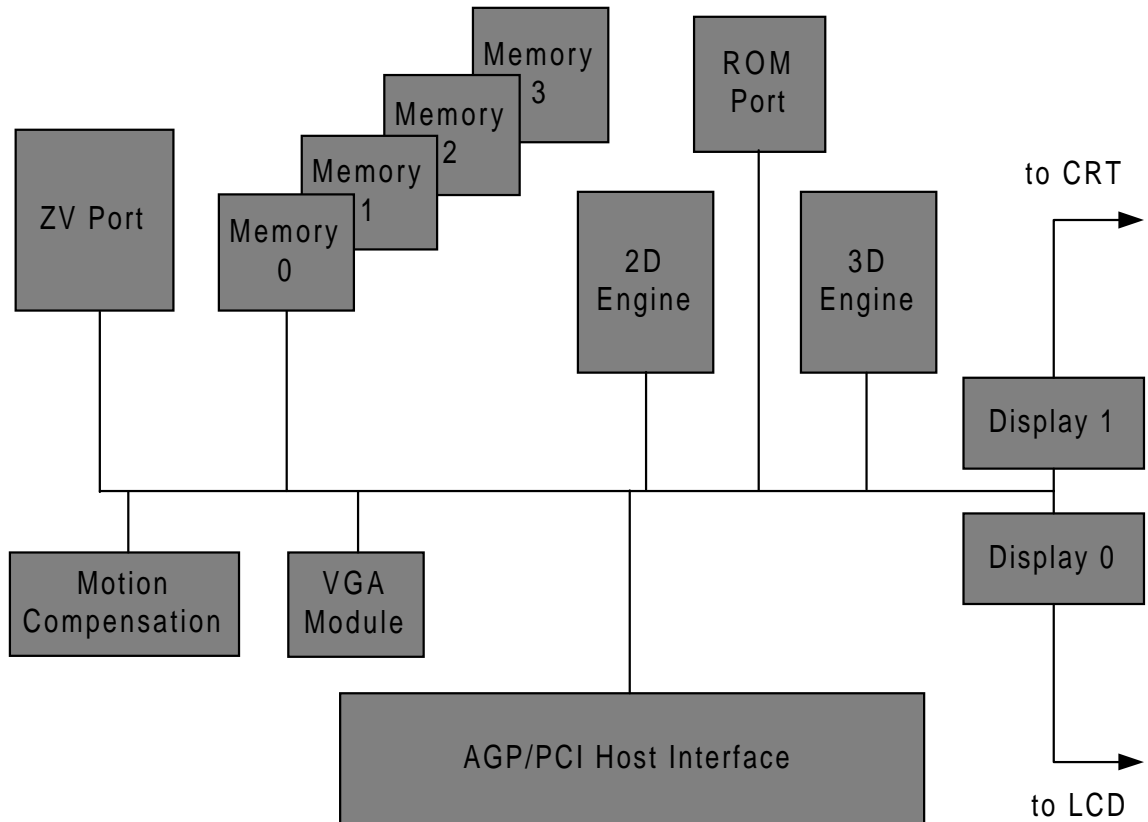
2.2　Internal Configuration

Figure 2-2. SM3110 Internal View

The architecture consists of a host interface, a standard VGA module, a Zoom Video port, a ROM port, four 1MB modules of high performance embedded memory, a 2D engine, a 3D engine, a motion compensation module for accelerating MPEG-2 playback and sophisticated dual display circuitry to support single/simultaneous/dual display on any LCD panel/CRT monitor/TV combination.
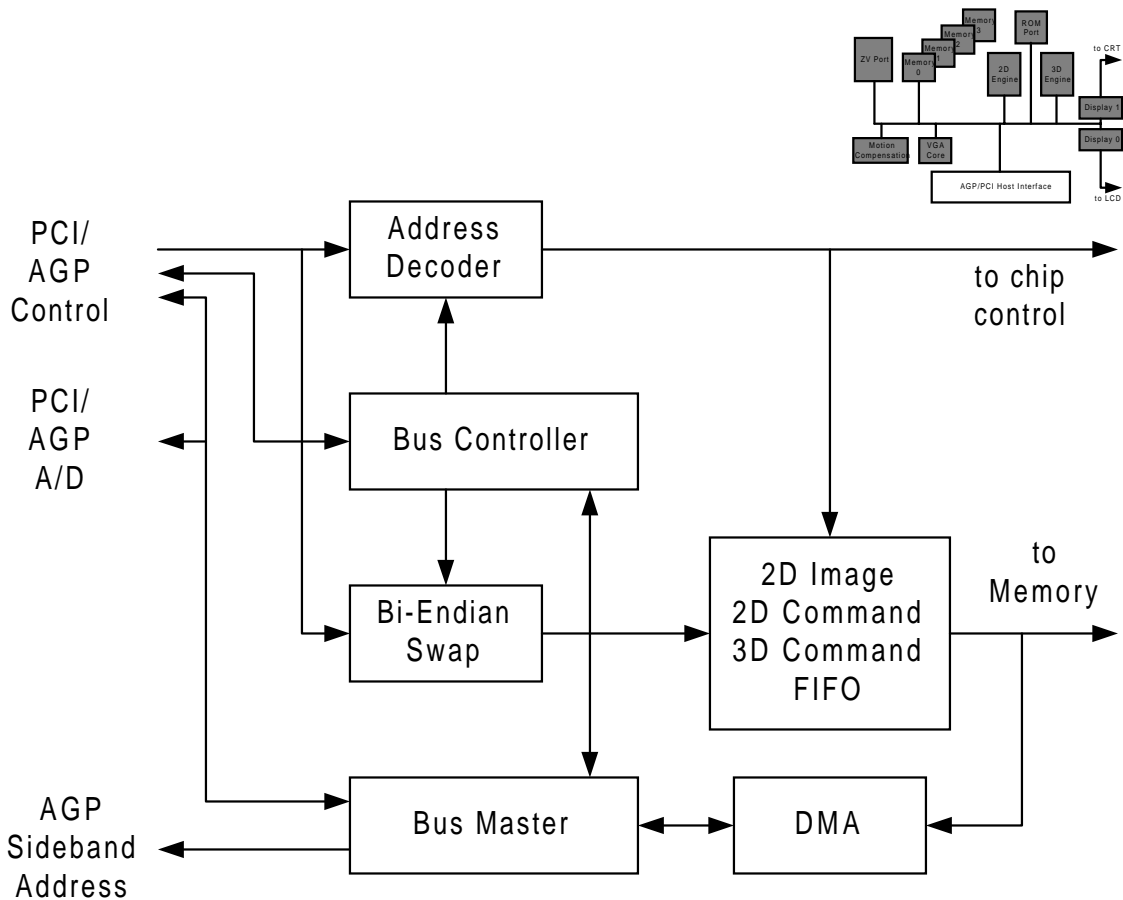
2.2.1 Host Interface

Figure 2-3. Host Interface

The SM3110 has a glueless system interface that is compliant with PCI Local Bus, Revision 2.2 and supports Intel's Accelerated Graphics Port (AGP), Revision 2.0. The system interface can initiate bus transactions as a master and supports 5V and 3.3V signaling and 66 MHz operation. It supports PCI Bus Power Management Interface for ACPI compliant power management. AGP support includes AGP 1x and 2x with Local Texturing, AGP Pipelining, AGP Sideband Addressing, and AGP Frame Mode.

The host interface supports bi-endian data formats. It has 2D and 3D command/data buffers to improve bus throughput. It handles DMA in bus master mode to improve data transfer while leaving the CPU free for other tasks. In AGP configuration the host interface also supports sideband addressing for higher data throughput.
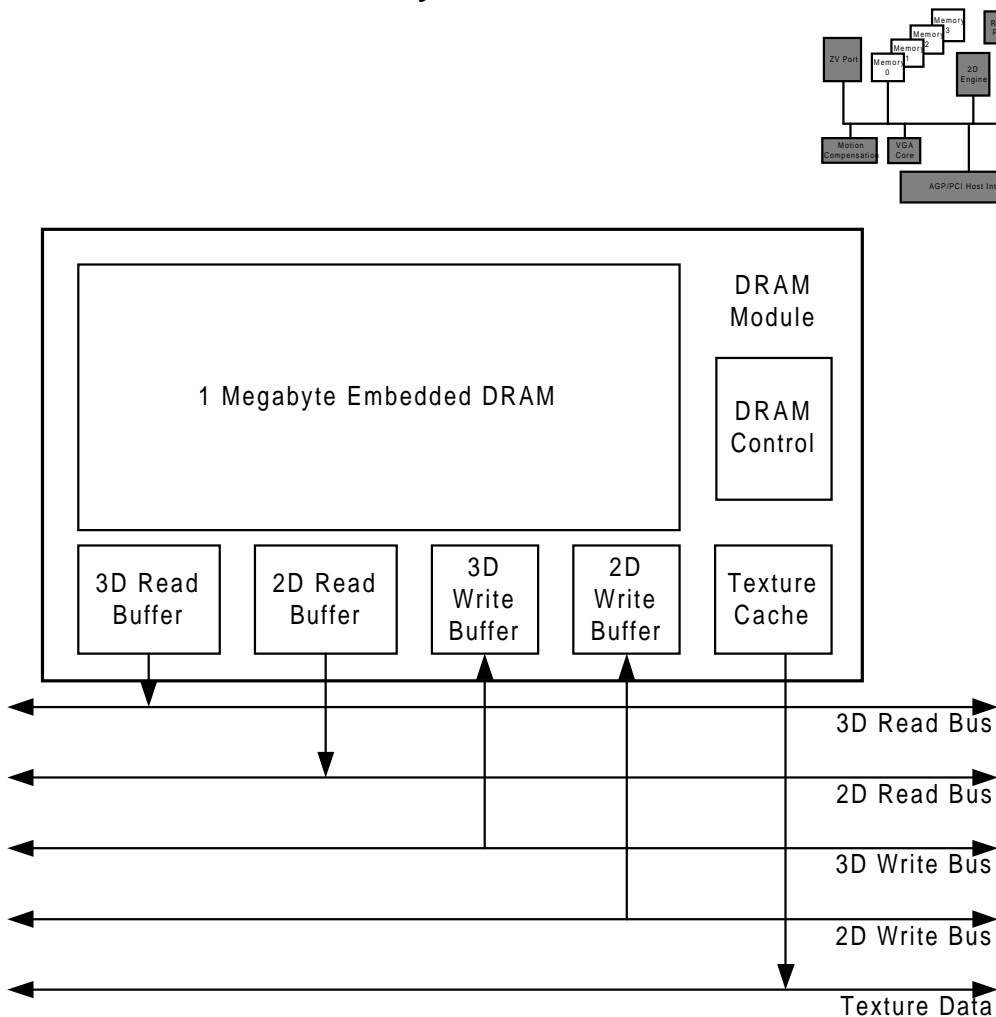
2.2.2 Embedded Memory

Figure 2-4. Memory Module Internal Path

The SM3110 includes 4 megabytes of embedded memory. Four memory modules of 1 megabyte each comprise the internal memory. The modules have separate read and write buffers for the 2D and 3D data buses and one buffer for texture cache. When combined, the interface to internal memory provides over 6.4 gigabytes/second peak memory bandwidth.

The SM3110 claims 128MB of memory space through AGP/PCI configuration. This 128 megabytes is divided into 4 contiguous 32MB address ranges. The lowest 32MB is for little endian data. The next 32MB is reserved. The swap byte within doubleword big endian copy occupies the next 32MB and the swap bytes within word big endian copy occupies the highest 32MB. The last 256KB of each 32MB address range is reserved for 2D and 3D control accesses.

Table 2-1. Local Address Space Allocation

Range	*Size*	Little Endian *Base*	Reserved *Base*	Big Endian (Double-Word Swap) *Base*	Big Endian (Word Swap) *Base*
Display Memory	31.75MB	00000000H	02000000H	04000000H	06000000H
Control	0.25MB	01FC0000H	03FC0000H	05FC0000H	07FC0000H
Total	32.00MB				

Besides the memory address mentioned above, SM3110 also provides access to register I/O and 128KB memory at 000A0000H address space for compatibility with standard VGA. Larger physical memory available in super VGA configuration is made accessible via an I/O addressed bank offset register.
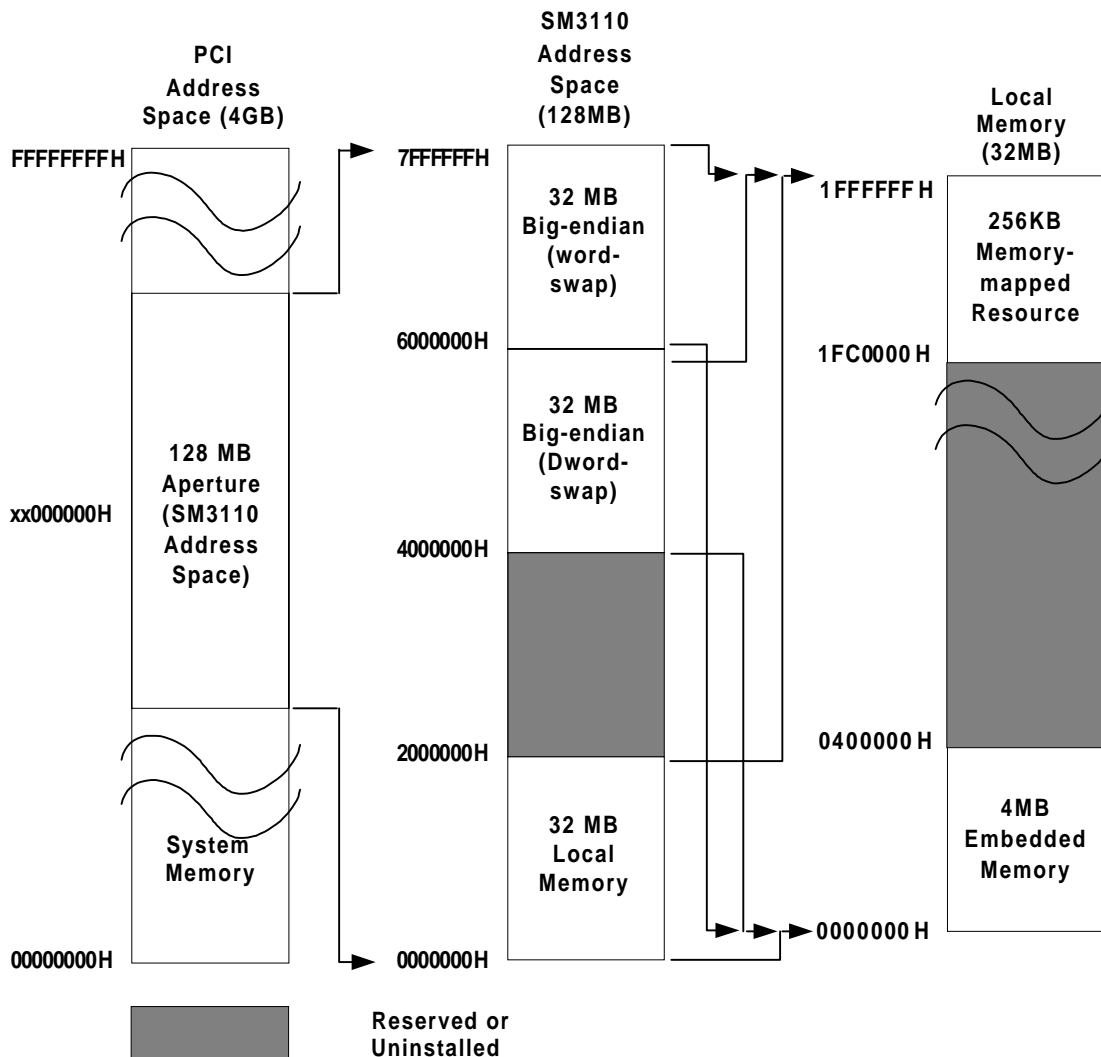
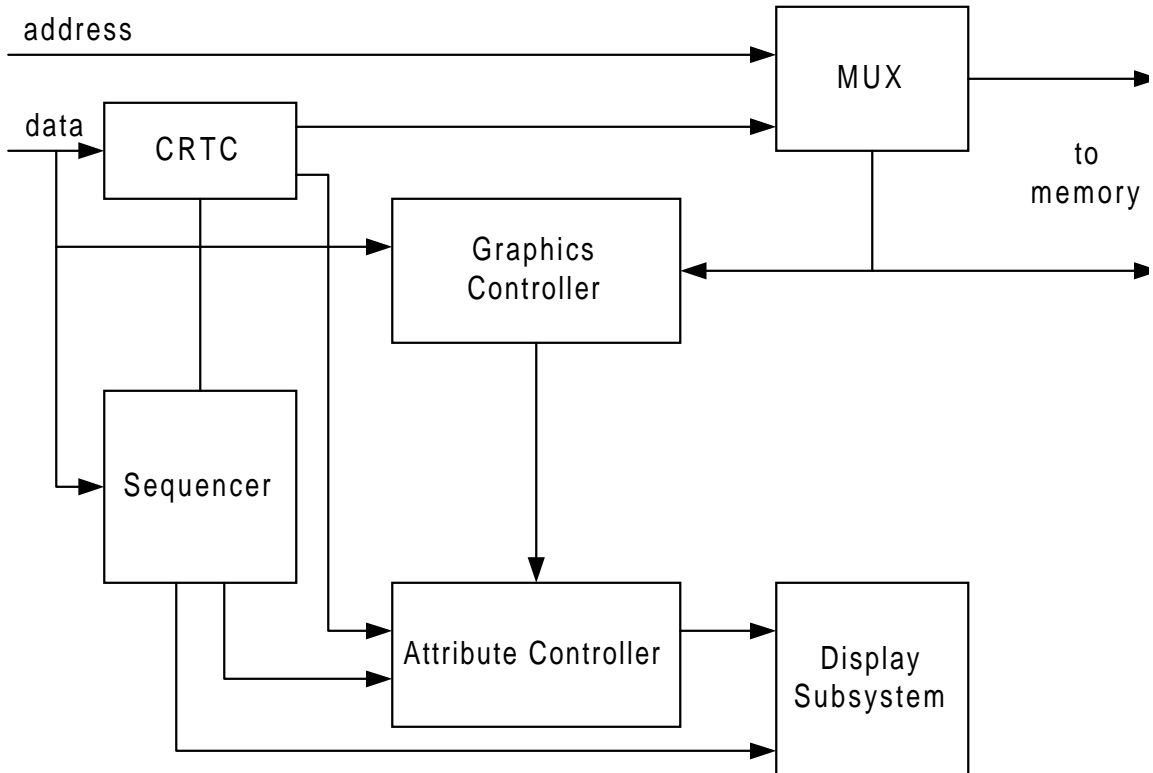**Figure 2-5. Address Space Allocation**
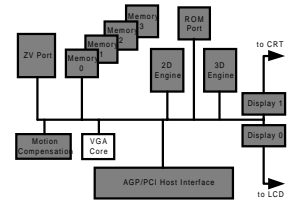
2.2.3   VGA Module

Figure 2-6. VGA Module

SM3110 has a VGA core fully compatible with the industry-standard IBM VGA adapter. This module provides direct access logic to the frame buffer and supports all functions performed by the Sequencer and VGA Graphics Controller registers. Standard VESA and VGA display timings are also provided by this module.
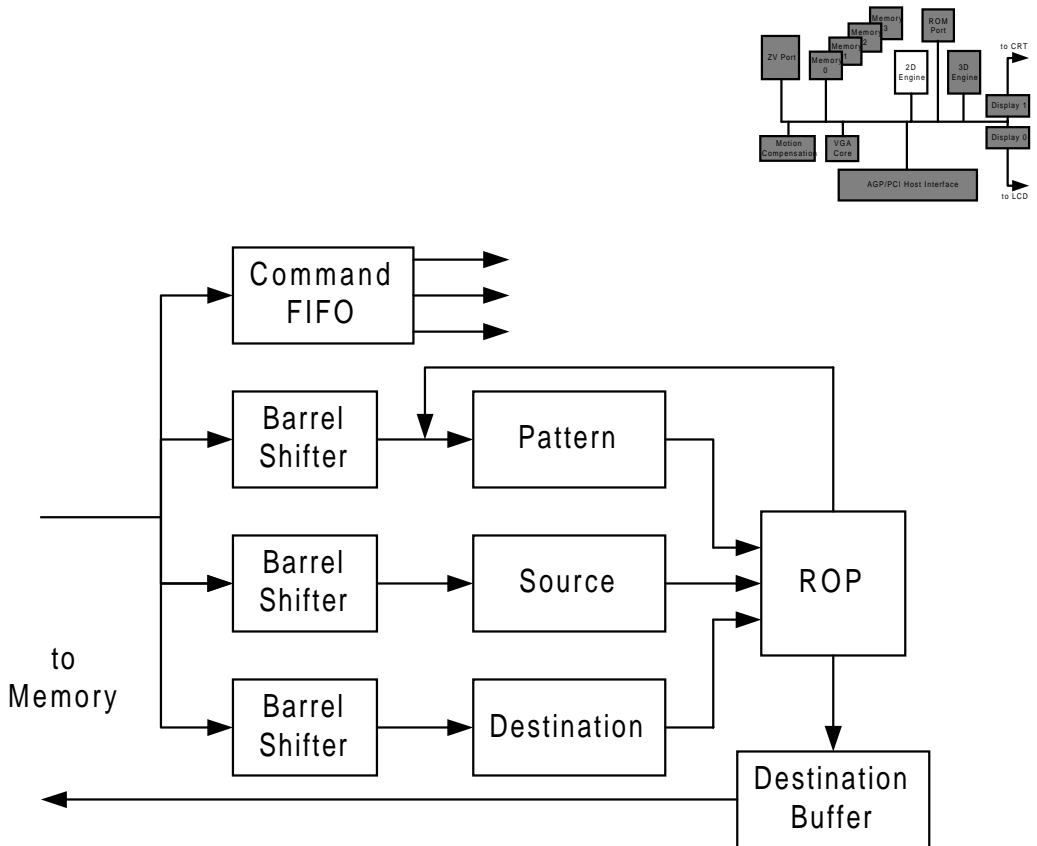
2.2.4 2D Rendering Engine

Figure 2-7.   2D BitBLT Engine Internal Data Path

The SM3110 has a high performance 2D bitBLT engine. The 2D engine has a three-operand raster operations (ROP) engine supporting linear and rectangular addressing which is fully Microsoft Windows compatible. It also supports screen-to-screen or memory-to-screen bitBLT with color expansion and transparency control.

The 2D command FIFO receives and decodes commands buffered for the 2D engine. Separate source data, destination data and pattern buffers have their own shifters to align data before they are fed into the ROP unit. A destination buffer stores the results before writing back to the frame buffer for optimized performance in both the 2D engine and the memory interface. This engine also provides transparency, color expansion and color keying during the bitBLT operation.
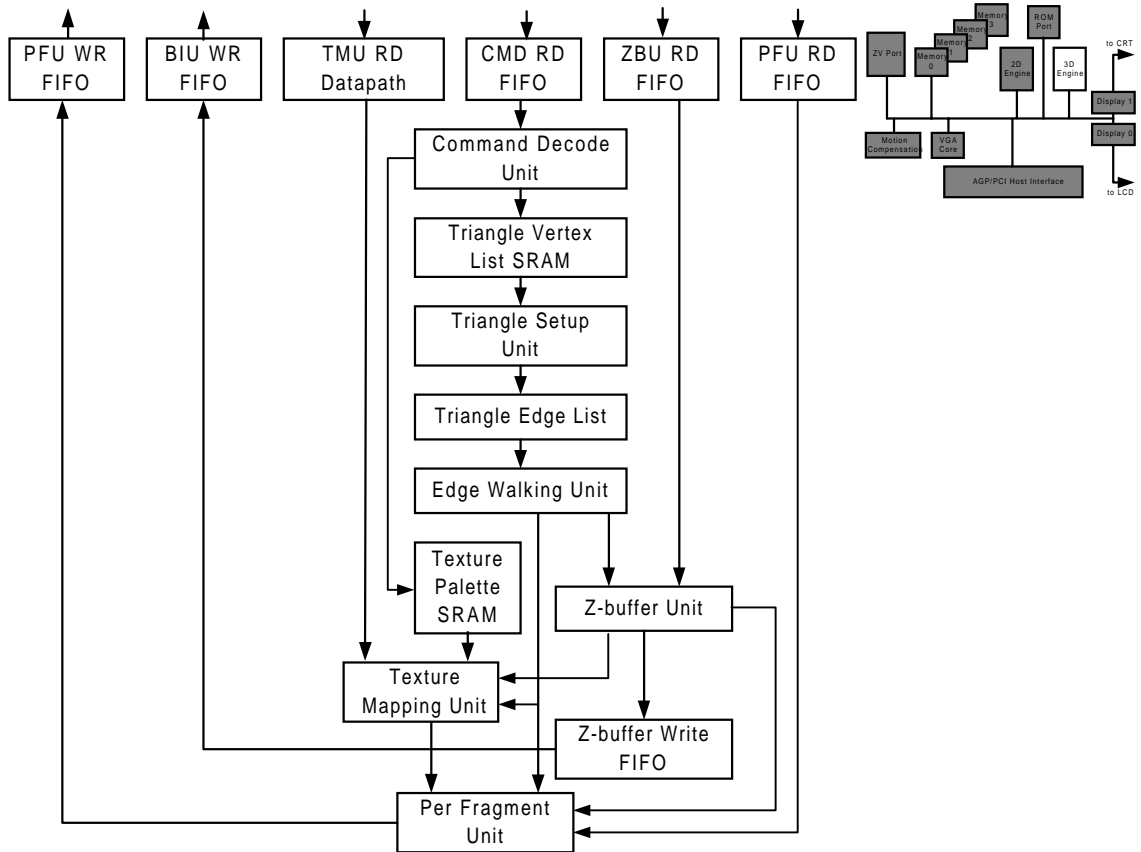
2.2.5 3D Rendering Engine

Figure 2-8. 3D Engine Internal Data Path

The SM3110 has a multi-stage 3D rendering engine. It is a one-cycle, bilinear, perspective corrected and two-cycle, trilinear, texture-mapped, perspective corrected MIPmap texture calculation engine. The major components of this rendering engine include a command unit, a triangle setup engine, a texture mapping unit, a texture cache buffer, a texture palette, a per fragment unit and a 16-bit Z-buffer.

The command unit provides command decoding and control of the engine. The triangle setup engine speeds up calculations in the setup process by getting setup information from the host and performing the necessary calculations, freeing the host CPU for other tasks. The texture unit calculates correct texels for each pixel with a bilinear or trilinear MIPmapped filter and perspective correction. The texture palette converts indexed color into 16-bit color. The Z-buffer unit calculates Z value of each new pixel and compares against the Z value in the frame buffer for accurate hidden surface removal. The rendering engine renders each pixel using lighting, fogging, specular highlighting and texturing functions to generate realistic images at a high frame rate.
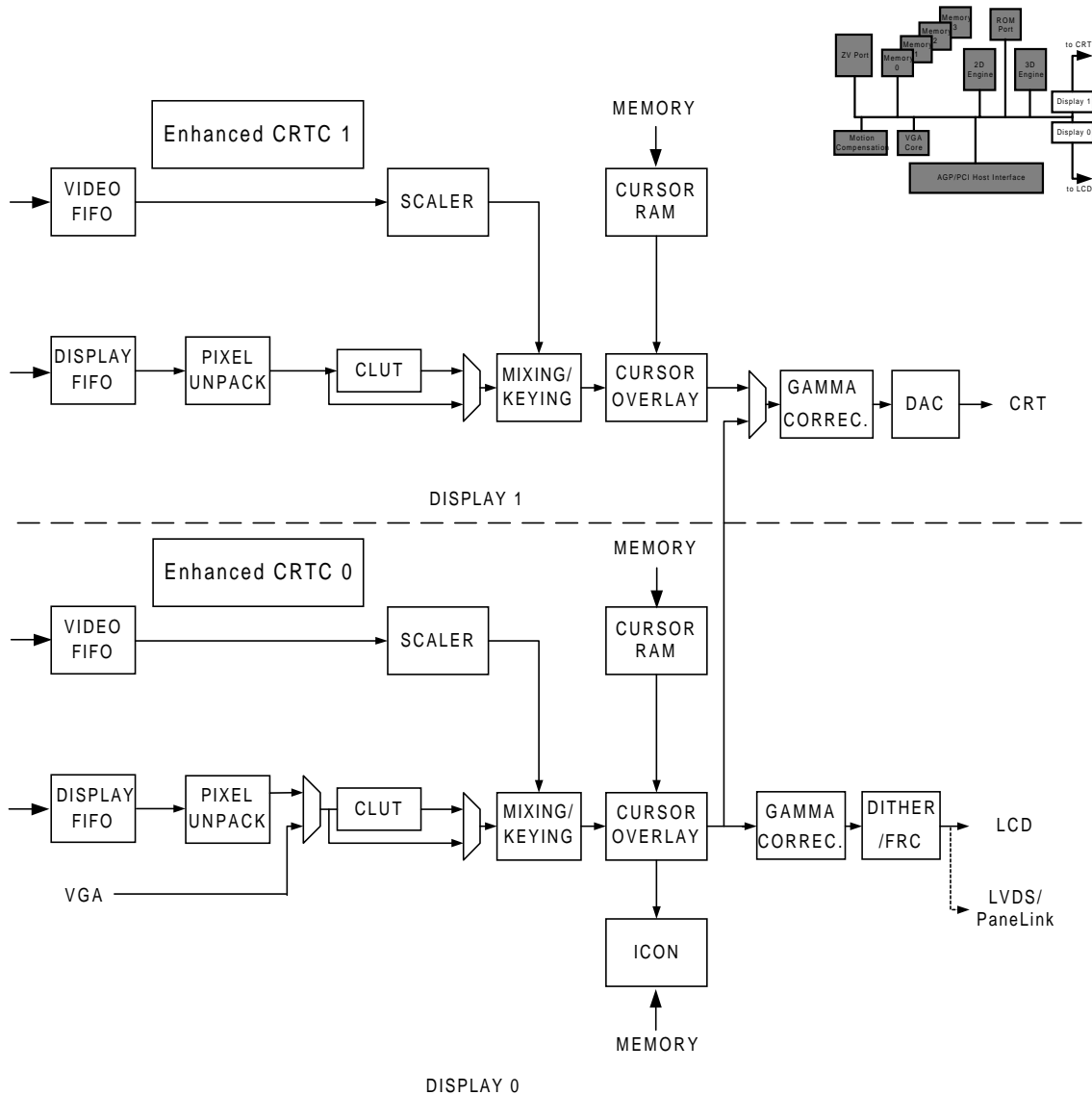
2.2.6 Display Pipeline

Figure 2-9. Display Pipeline

The display subsystem has two independent display pipelines. Each pipeline has its own enhanced CRT controller (CRTC), display FIFO, video FIFO, pixel unpacking circuit, color lookup table (CLUT), color keying circuit and scaler. Display 0 supports all standard VGA functions including all standard VESA display modes. Both displays support extended VESA modes for higher visual quality. The two enhanced CRT controllers can be set to display different data with different resolutions and refresh rates. Display 1 can accept display 0 data through a multiplexing circuit.

The last stages of the two pipelines differ somewhat. Display pipeline 0 is optimized for flat panel display with gamma correction. It has a software selectable dithering and Frame Rate Control (FRC) circuit to improve display quality on LCD panels. The same interface can also provide digital data to drive an external LVDS/PaneLink transmitter. It supports 8, 16, 24 and 36 pin interface DSTN panels with dithering and FRC. It also supports a 9, 12, 18, 24 and 36 pin interface TFT panels with dithering, and supports scaling and centering if the display resolution is lower than panel resolution. SM3110 also supports panning if the display resolution is larger than the panel resolution.

Display pipeline 1 integrates a true color 230 MHz palette DAC with gamma correction. It can display 4, 8, 15, 16, 24 and 32 bits per pixel (bpp) with standard VGA, VESA and programmable enhanced display formats up to 1600 by 1200 resolution at 85Hz. VESA Display Power Management Signaling 1.0 (DPMS 1.0) is supported for power management. The SM3110 also supports VESA Display Data Channel 2.0/2.0B (DDC2/DDC2B) for monitor Plug & Play support. The CRT can have display timing and control independent of the flat panel for dual independent displays.

The display subsystem supports two hardware cursors and a hardware icon. The size of both the cursors and icon is 32 pixels by 32 pixels in 8bpp color mode or 256 pixels by 256 pixels in monochrome mode. The cursors can be on both display pipelines, while the icon can only be on the display 0 pipeline.
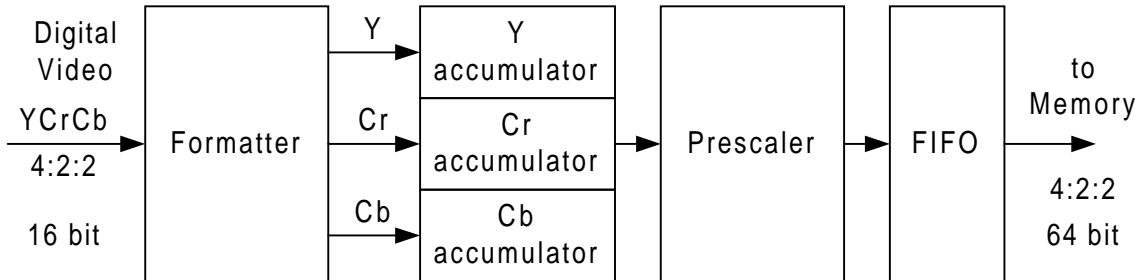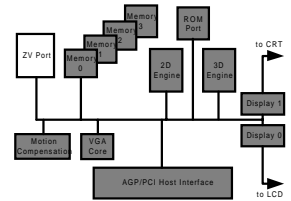
2.2.7 Video Input

Figure 2-10. Video Input

The SM3110 supports PCMCIA Zoomed Video (ZV) Port and direct video input of ITU-R BT. 601 compliant YCrCb 4:2:2 digital video data.

The video data from this port is first pixel-aligned by a formatter and put into an accumulator. When two complete pixels are accumulated, the decimator circuit prescales the data and writes the scaled result into the frame buffer through its own FIFO for video capture.
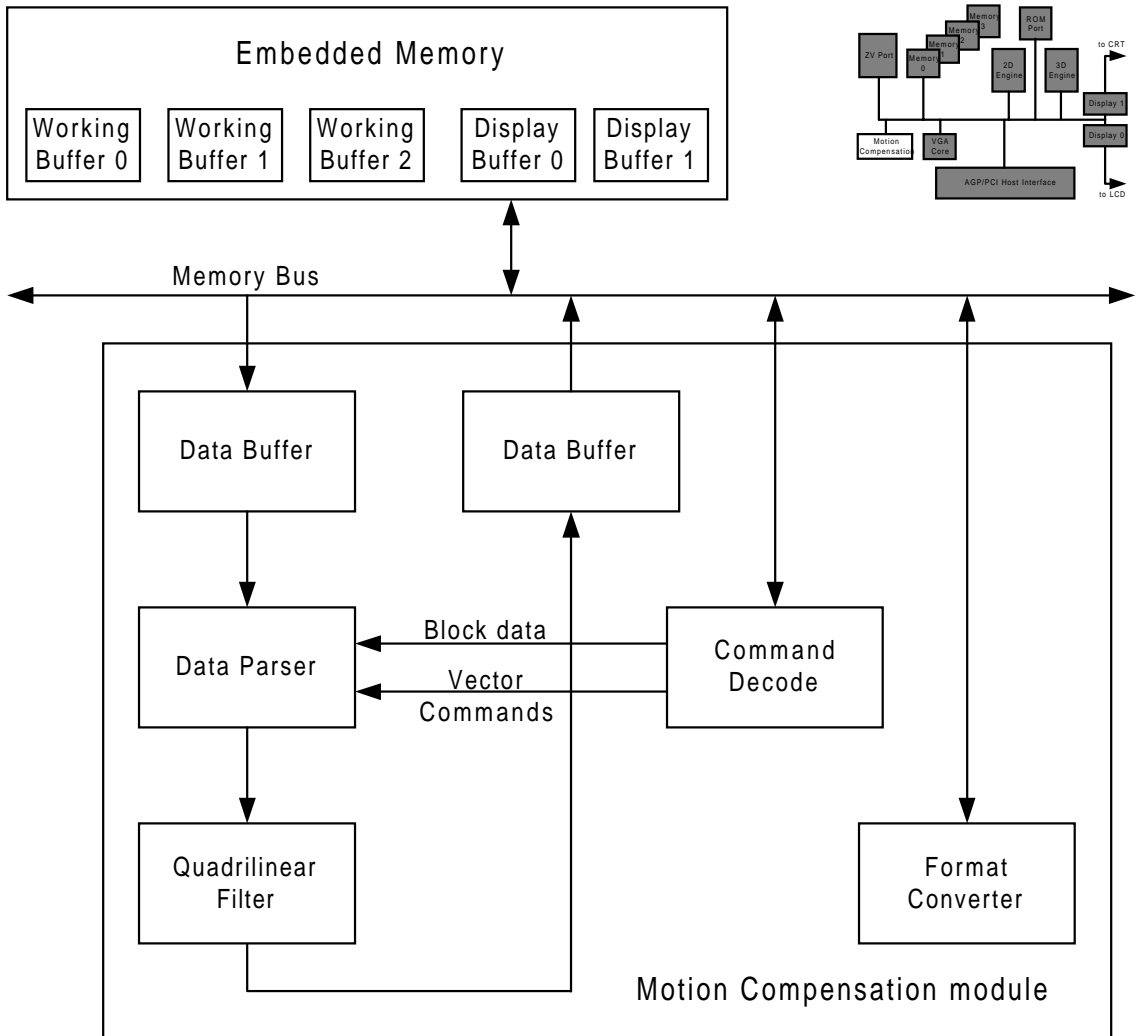
2.2.8 Motion Compensation

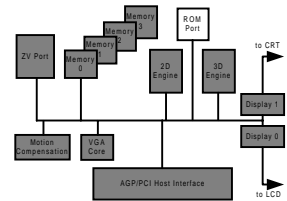**Figure 2-11. Motion Compensation Subsystem**

The motion compensation subsystem consists of the motion compensation module and five buffers residing in internal memory.   The motion compensation module accepts enhanced MPEG-2 video data, parses the macroblock data and applies the quadrilinear filter. The resulting picture is assembled in the working buffers and then converted on the fly from the input 4:2:0 YCrCb format to output 4:2:2 YCrCb format and written to the display buffer.

2.2.9   ROM Port

The SM3110 supports external display BIOS ROM in standard VGA
BIOS address 0xC000:0000. The ROM can be EPROM, EEPROM, or
flash ROM. The size is either 32KB or 64KB and is set by power-on
strapping.

If display BIOS is incorporated in system BIOS, this port can be converted to drive an external digital TV encoder. The image can be programmed to be the same as either the CRT or the panel display.

The ROM port can also be used for any 8-bit peripheral I/O function through the peripheral port at address offset +1FE0000H.

2.3 Additional Features

2.3.1 Power Management

The SM3110 supports PCI Bus Power Management Interface for ACPI compliant power management, VESA Display Power Management Signaling 1.0 (DPMS 1.0) and VESA Display Data Channel 2.0/2.0B (DDC2/DDC2B) for monitor Plug & Play support.

The panel interface, DAC, 2D engine, 3D engine, both scalers and the entire display 1 (CRT) pipeline can be turned off individually to tailor the chip configuration for the lowest power consumption. The SM3110 allows the lowest possible power use dynamically through driver/register-level control for the task at hand.

2.3.2 Board-level Test Functions

The SM3110 has build-in test functions to perform open/short connection testing to help in detecting manufacturing problems. This simple, effective method allows quick detection of any shorted connections or failed soldering. SM3110 also has an isolation test function which allows the board to be tested without response from the SM3110.

2.3.3 Clocks

The SM3110 has 3 internal clock synthesizers which provide a wide range of frequencies to the memory clock and the two display clocks. The inputs of the synthesizers are from a single clock source, which can be an oscillator or a crystal. The typical frequency is 14.31818 MHz.

2.3.4 Inter-IC (I^2C) Interface

The SM3110 has 8 programmable bi-directional pins to support I^2C and other control functions. Two sets of pins are provided to support DDC2B monitor control and a TV decoder/encoder for video in/TV out functions. More channels can be provided if the need arises.