

69000

In-Circuit Test Mode
Analysis for the
HiQVPro™ Controller

Application Note
Revision 1.0

June 1998

P R E L I M I N A R Y



A SUBSIDIARY OF INTEL CORPORATION

Copyright Notice

Copyright© 1998 Chips and Technologies, Inc., a subsidiary of Intel Corporation, ALL RIGHTS RESERVED.

This manual is copyrighted by Chips and Technologies, Inc., a subsidiary of Intel Corporation. You may not reproduce, transmit, transcribe, store in a retrieval system, or translate into any language or computer language, in any form or by any means - electronic, mechanical, magnetic, optical, chemical, manual, or otherwise - any part of this publication without the express written permission of Chips and Technologies, Inc., a subsidiary of Intel Corporation.

Restricted Rights Legend

Use, duplication, or disclosure by the Government is subject to restrictions set forth in subparagraph (c)(1)(ii) of the Rights in Technical Data and Computer Software clause at 252.277-7013.

Trademark Acknowledgment

CHIPS Logo is a registered trademark of Chips and Technologies, Inc., a subsidiary of Intel Corporation.

HiQVideo, is a trademark of Chips and Technologies, Inc., a subsidiary of Intel Corporation.

All other trademarks are the property of their respective holders.

Disclaimer

This document provides general information for the customer. Chips and Technologies, Inc., a subsidiary of Intel Corporation, reserves the right to modify the information contained herein as necessary and the customer should ensure that it has the most recent revision of the document. CHIPS makes no warranty for the use of its products and bears no responsibility for any errors which may appear in this document. The customer should be on notice that many different parties hold patents on products, components, and processes within the personal computer industry. Customers should ensure that their use of the products does not infringe upon any patents. CHIPS respects the patent rights of third parties and shall not participate in direct or indirect patent infringement.

Revision History

<u>Revision</u>	<u>Date</u>	<u>By</u>	<u>Comment</u>
0.1	5/21/98	DJ/Inc	Initial Release.
1.0	5/29/98	DJ/Inc	Formatting for useability.

Table of Contents

1.0 Introduction	1
2.0 Operation	1
Timing Diagram for ICT Mode	1
NAND Gate Chain for the 69000	2
BGA Pin Diagram for the 69000	3
3.0 Command File Programs	4
Sequence of the NAND Gate Chain	4

In-Circuit Test Mode Analysis for the HiQVideo™ Series Controllers

1.0 Introduction

The In-Circuit Test (ICT) Mode for the HiQVideo Series of graphics controllers is a state where all digital pins except RCLK, STNDBY# and the power and ground pins may be tested individually to determine if they are properly connected. This application note provides the details on how the controller works in this mode.

2.0 Operation

- 1) Pull all pins high except RCLK, STNDBY# and power and ground pins.
- 2) Pull RESET and RMD4 low.
- 3) Toggle the RCLK pin twice to high. This will start the test mode as shown in Figure 1, line A. Stop pulsing after the second pulse.
- 4) Pull RESET and RMD4 high. When the RESET goes low again, you are ready to test the individual pins (see line B in Figure 1).
- 5) Toggle the pins low one at a time starting with CFG0 (D18) as shown in Figure 1, lines C, D and E in the order given in Table 1. The VSYNC pin will toggle with each pin tested.
- 6) If VSYNC fails to toggle when any pin is pulled low, the pin is not connected or is somehow defective.

For proper operation of the in-circuit test and as a safety precaution, everything not on the ring-down list (Table 1) should be pulled high.

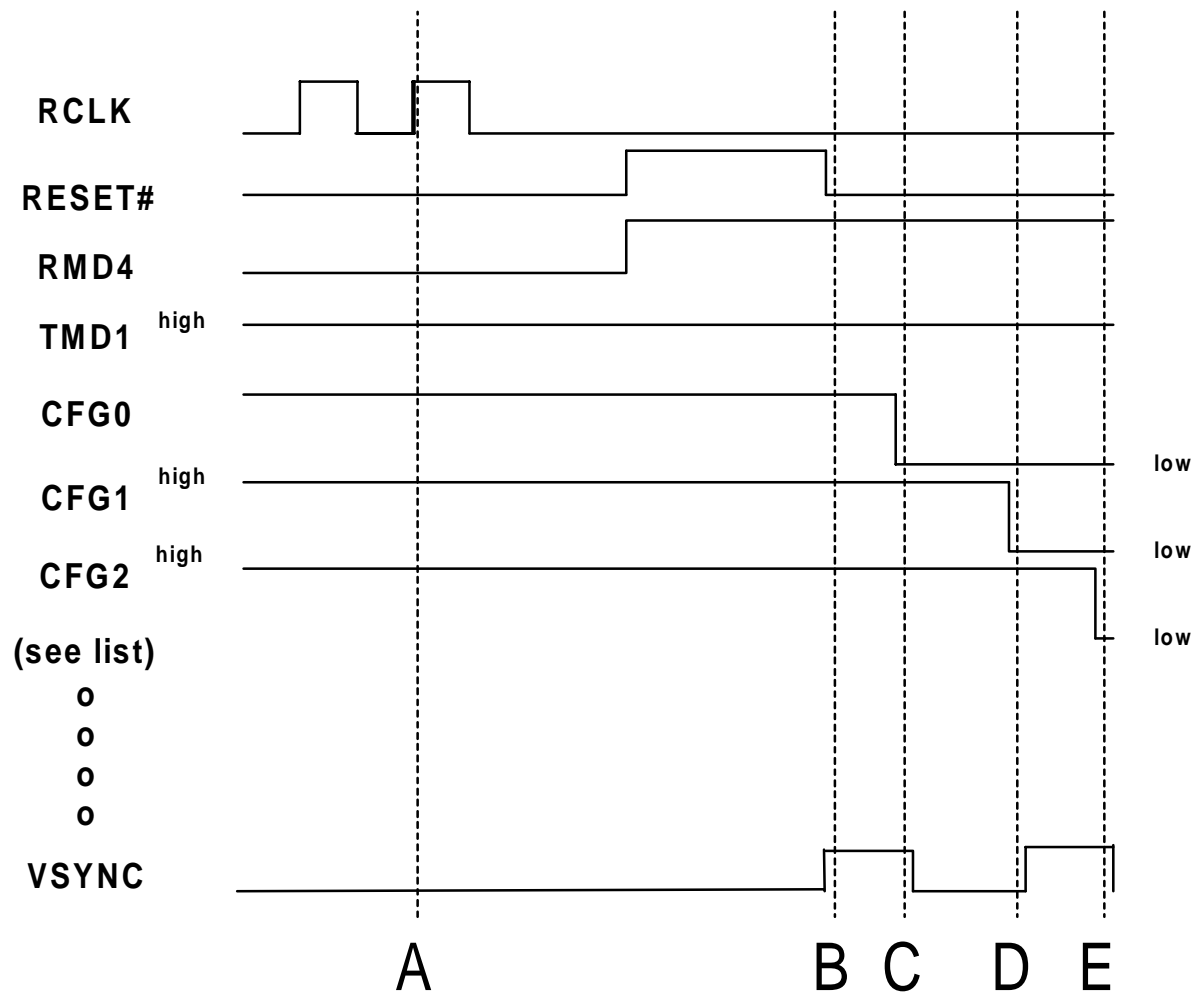


Figure 1: Timing Diagram for ICT Mode

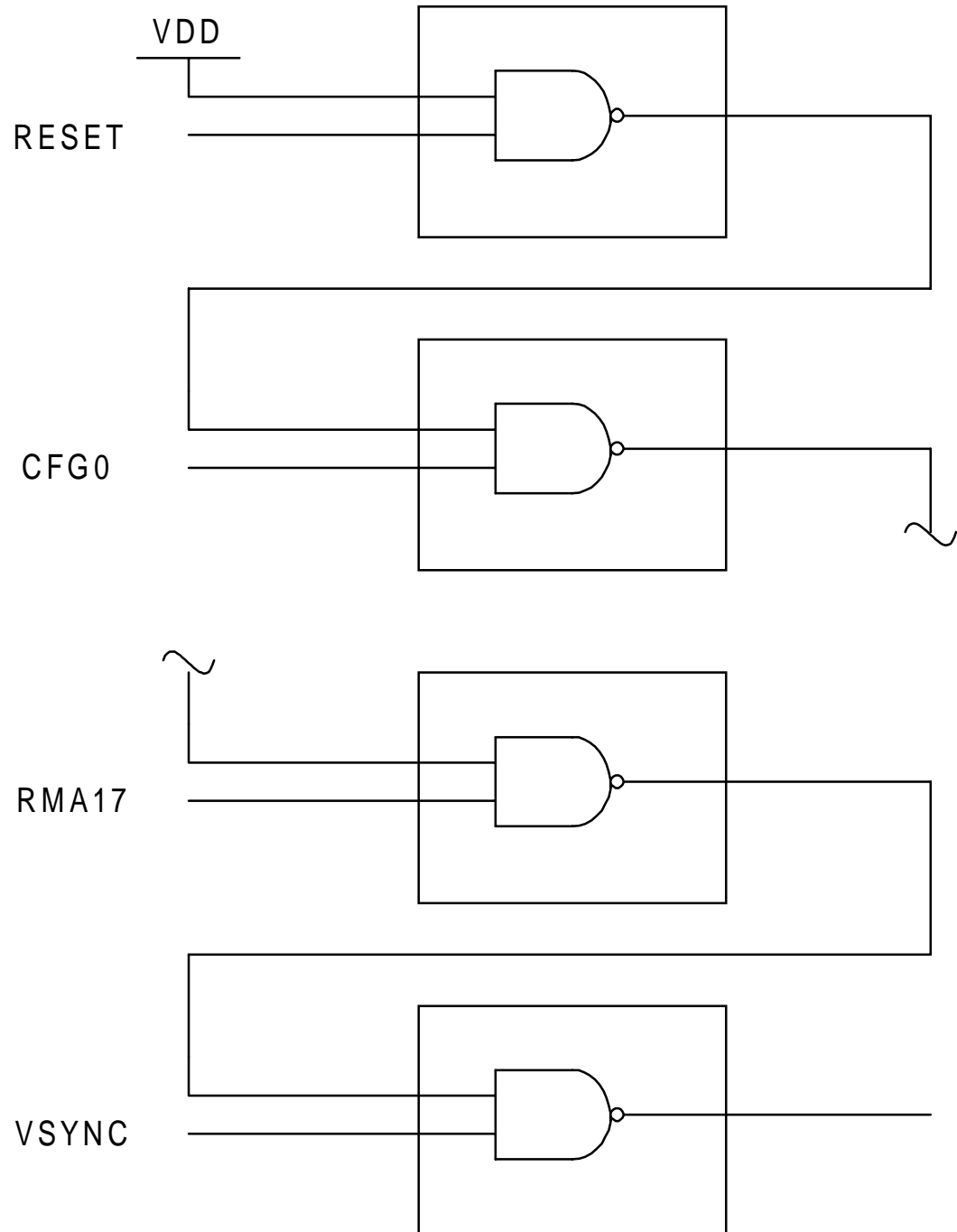


Figure 2: NAND Gate Chain for the 69000

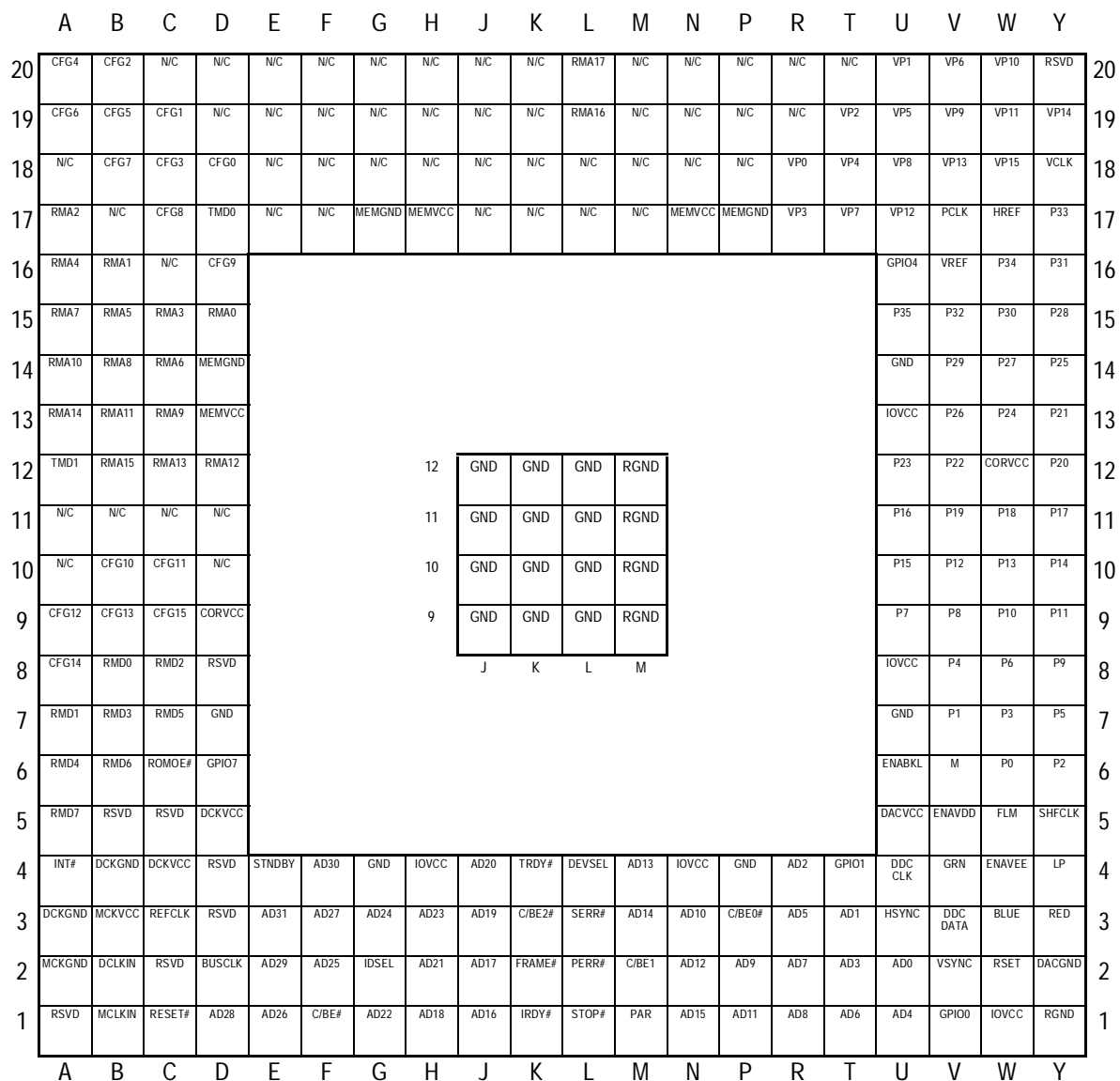


Figure 3: BGA Pin Diagram for 69000 (Top View)

Table 1: The sequence of the NAND gate chain.

Seq	Name (Ball)	Seq	Name (Ball)	Seq	Name (Ball)	Seq	Name (Ball)
1	RESET# (CI)	41	BCLK (D2)	81	AD5 (R3)	121	P23 (U12)
2	CFG0 (D18)	42	AD31 (E3)	82	AD4 (U1)	122	P24 (W13)
3	CFG1 (C19)	43	AD30 (F4)	83	AD3 (T2)	123	P25 (Y14)
4	CFG2 (B20)	44	AD29 (E2)	84	AD2 (R4)	124	P26 (V13)
5	CFG3 (C18)	45	AD28 (D1)	85	AD1 (T3)	125	P27 (W14)
6	CFG4 (A20)	46	AD27 (F3)	86	AD0 (U2)	126	P28 (Y15)
7	CFG5 (B19)	47	AD26 (E1)	87	GPIO0 (T4)	127	P29 (V14)
8	CFG6 (A19)	48	AD25 (F2)	88	GPIO1 (H2)	128	P30 (W15)
9	CFG7 (B18)	49	AD24 (G3)	89	GPIO2 (V3)	129	P31 (Y16)
10	CFG8 (C17)	50	BE3 (F1)	90	GPIO3 (U4)	130	P32 (V15)
11	CFG9 (D16)	51	IDSEL (G2)	91	ENAVEE (W4)	131	P33 (Y17)
12	RMA0 (D15)	52	AD23 (H3)	92	ENAVDD (V5)	132	P34 (W16)
13	RMA1 (B16)	53	AD22 (G1)	93	ENABKL (U6)	133	P35 (U15)
14	RMA2 (A17)	54	AD21 (H2)	94	FLM (W5)	134	VREF (V16)
15	RMA3 (C15)	55	AD20 (J4)	95	LP (Y4)	135	HREF (W17)
16	RMA4 (A16)	56	AD19 (J3)	96	M (V6)	136	VCLK (Y18)
17	RMA5 (B15)	57	AD18 (H1)	97	SHFCLK (Y5)	137	GPIO4 (U16)
18	RMA6 (C14)	58	AD17 (J2)	98	P0 (W6)	138	PCLK (V17)
19	RMA7 (A15)	59	AD16 (J1)	99	P1 (V7)	139	VP15 (W18)
20	RMA8 (B14)	60	BE2 (K3)	100	P2 (Y6)	140	VP14 (Y19)
21	RMA9 (C13)	61	FRAME# (K2)	101	P3 (W7)	141	VP13 (V18)
22	RMA10 (A14)	62	IRDY# (K1)	102	P4 (V8)	142	VP12 (U17)
23	RMA11 (B13)	63	TRDY# (K4)	103	P5 (Y7)	143	VP11 (W19)
24	RMA12 (D12)	64	DEVSEL# (L4)	104	P6 (W8)	144	VP10 (W20)
25	RMA13/CFG11 (C12/C10)	65	STOP (L1)	105	P7 (U9)	145	VP9 (V19)
26	RMA14/CFG12 (A13/A9)	66	PERR# (L2)	106	P8 (V9)	146	VP8 (U18)
27	RMA15/CFG10 (B12/B10)	67	SERR# (L3)	107	P9 (Y8)	147	VP7 (T17)
28	GPIO5 (N18) *	68	PARITY (M1)	108	P10 (W9)	148	VP6 (V20)
29	GPIO7 (P20)	69	BE1 (M2)	109	P11 (Y9)	149	VP5 (U19)
30	RMD0/CFG13 (B8/B9)	70	AD15 (N1)	110	P12 (V10)	150	VP4 (T18)
31	RMD1/CFG12 (A7/A8)	71	AD14 (M3)	111	P13 (W10)	151	VP3 (R17)
32	RMD2/CFG15 (C8/C9)	72	AD13 (M4)	112	P14 (Y10)	152	VP2 (T19)
33	RMD3/TM0 (B7/D17)	73	AD12 (N2)	113	P15 (U10)	153	VP1 (U20)
34	RMD4/TM1 (A6/A12)	74	AD11 (P1)	114	P16 (U11)	154	VP0 (R18)
35	RMD5 (C7)	75	AD10 (N3)	115	P17 (Y11)	155	RMA16 (L19)
36	RMD6 (B6)	76	AD9 (P2)	116	P18 (W11)	156	RMA17 (L20)
37	RMD7 (A5)	77	AD8 (R1)	117	P19 (V11)	157	HSYNC (U3)
38	ROMOE# (C6)	78	BE0 (P3)	118	P20 (Y12)	158	VSYSN (V2)
39	TMD0 (D17)	79	AD7 (R2)	119	P21 (Y13)	159	
40	INT# (A4)	80	AD6 (T1)	120	P22 (V12)	160	

* GPIO5 (ball N18) is listed as 'NC' in the pin diagram. It must be connected for the in-circuit test to work properly.



A SUBSIDIARY OF INTEL CORPORATION

Chips and Technologies, Inc.
a subsidiary of Intel Corporation
2950 Zanker Road
San Jose, California 95134
Phone: 408-434-0600
FAX: 408-894-2077

Title:	69000 ICT
Publication No.:	AN120
Stock No.:	020120-000
Revision No.:	1.0
Date:	6/05/98