DK6555X-PCI

(Fab Rev. E)

HiQVideo™ Series
PC Board Design Documentation

User's Guide
Revision 1.1

February 1997

P R E L I M I N A R Y

Revision History

Revision	Date	By	Comment
1.0	1/24/97	DJ/lc	Initial Release for Fab Rev E boards.
1.1	2/11/97	DJ/lc	Added references for using a 65555 on a 65554 daughter card.

Table of Contents

List of Tables

List of Figures

DK6555X PCI (Fab Rev. E)
PCB Design Documentation

1.0 PRODUCT DESCRIPTION

The HiQVideo™ Series accelerators (6555X, 6855X, and successor products) are very high performance LCD/CRT controllers that provide a complete video sub-system solution with low power consumption, hardware acceleration for GUI applications, and a minimal component count. The high level of integration permits a direct interface to the PCI Bus and DRAM based display memory, thus making the HiQVideo™ controller a low cost, high performance graphics solution.

The design kits for these products in the PCI Bus environment all utilize a common base board known as the DK6555X PCI DK Board. A daughter card containing the HiQVideo controller is installed onto the main DK board to complete the design kit. This User Guide describes the 65550 and 65554 Daughter Cards as well as the main DK board. The usage of a 65555 HiQVideo accelerator on a 65554 Daughter Card is also described in this User Guide. Daughter cards for all other products are described in separate User Guide documents.

The DK6555X PCI board is a full size AT add-in card. It has bus connectors to interface with the PCI Bus at speeds up to 33MHz. The multiple jumper configurations and connectors allow the DK board to test performance benchmarks, demonstrate various features supported by the HiQVideo™ family, measure power consumption, and connect to panels and monitors. Plug-and-Play is possible on the PCI Bus, thus making PCI easy to use. The PCI auto-configuration feature determines interrupt setting and software defaults. The HiQVideo™ VGA controllers are mounted on a daughter card which plugs into a connector on the DK6555X PCI board to make a complete design kit. This allows the user to exchange silicon simply by replacing the daughter card without having to replace the entire kit.

This document describes the revision "E" of the DK6555X PCI printed circuit board. Revision "E" boards may be identified by copper "Fab Rev E" markings on the soldered side of the board between J7 and J9.

1.1 Using a 65555 device on a 65554 Daughter Card

Throughout this document, except where otherwise specified, all references to the 65554 Daughter Card also apply when a 65555 HiQVideo controller is mounted on the daughter card instead of a 65554.

IMPORTANT: The 65555 requires all of its VCC pins to be at 3.3V. To avoid possible damage to the 65555, the VCC jumpers on the main DK board must be set to provide 3.3V rather than 5V to the 65555. See Section 6.20 for a complete example of how to set all jumpers for use with a 65555 HiQVideo controller.

2.0 FEATURES

The DK6555X board has the following features when running a HiQVideo™ controller:

- High Performance Flat Panel/CRT GUI Accelerator running on PCI Bus
- Flexible display memory configurations support up to 4MB with a 65554, and 2MB with 65550. The memory resides on the daughter card.
- 50-pin flat panel connector for interfacing to most types of flat panels (up to 24 data bits)
- 26-pin flat panel connector for 12 additional data bits for panels having up to a 36-bit data word width
- 15-pin standard VGA connector
- 40-pin MPEG connector for interfacing to an MPEG video card
- Two 25-pin and one 12-pin connector for interfacing to the multimedia daughter card.

  (A multimedia daughter card can be purchased separately by ordering part number MM6555x Multimedia Daughter Card.)
- PCI BIOS ROM support, located on the daughter card.
- Flexible power supplies individually configurable to 3.3V and 5V for different blocks of the video subsystem
- On board power sequencing
- VGA to NTSC/PAL conversion to provide S-VHS video and composite video outputs

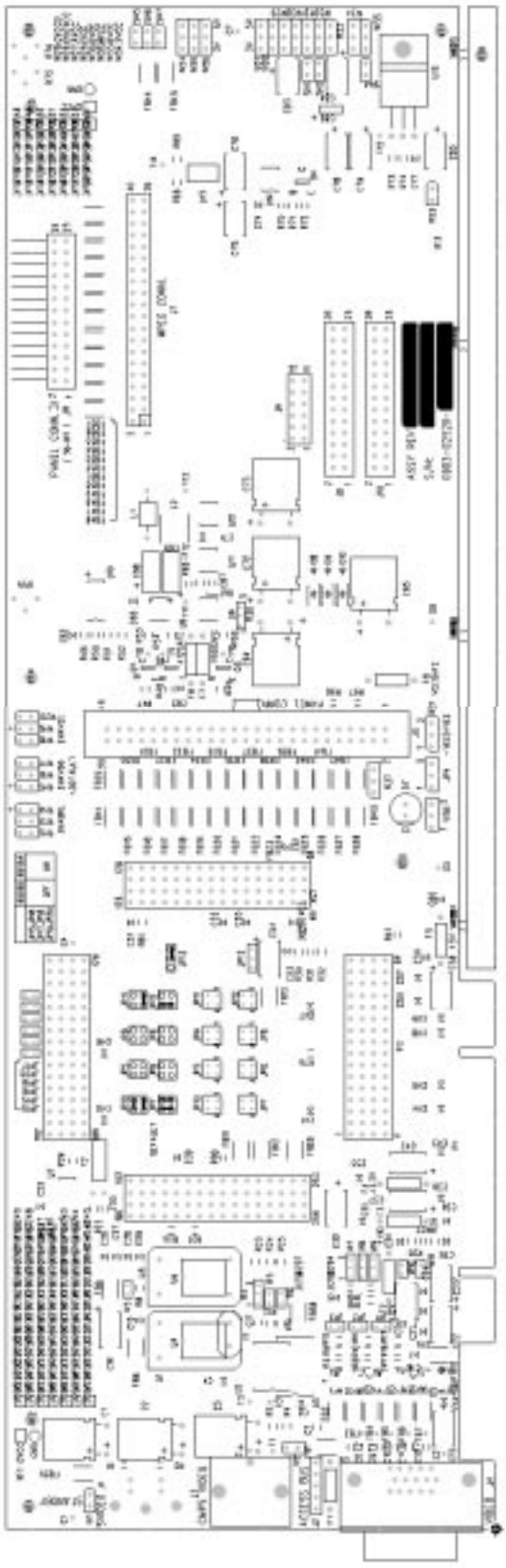

Figure 1: DK6555X PCI Board Layout Rev E

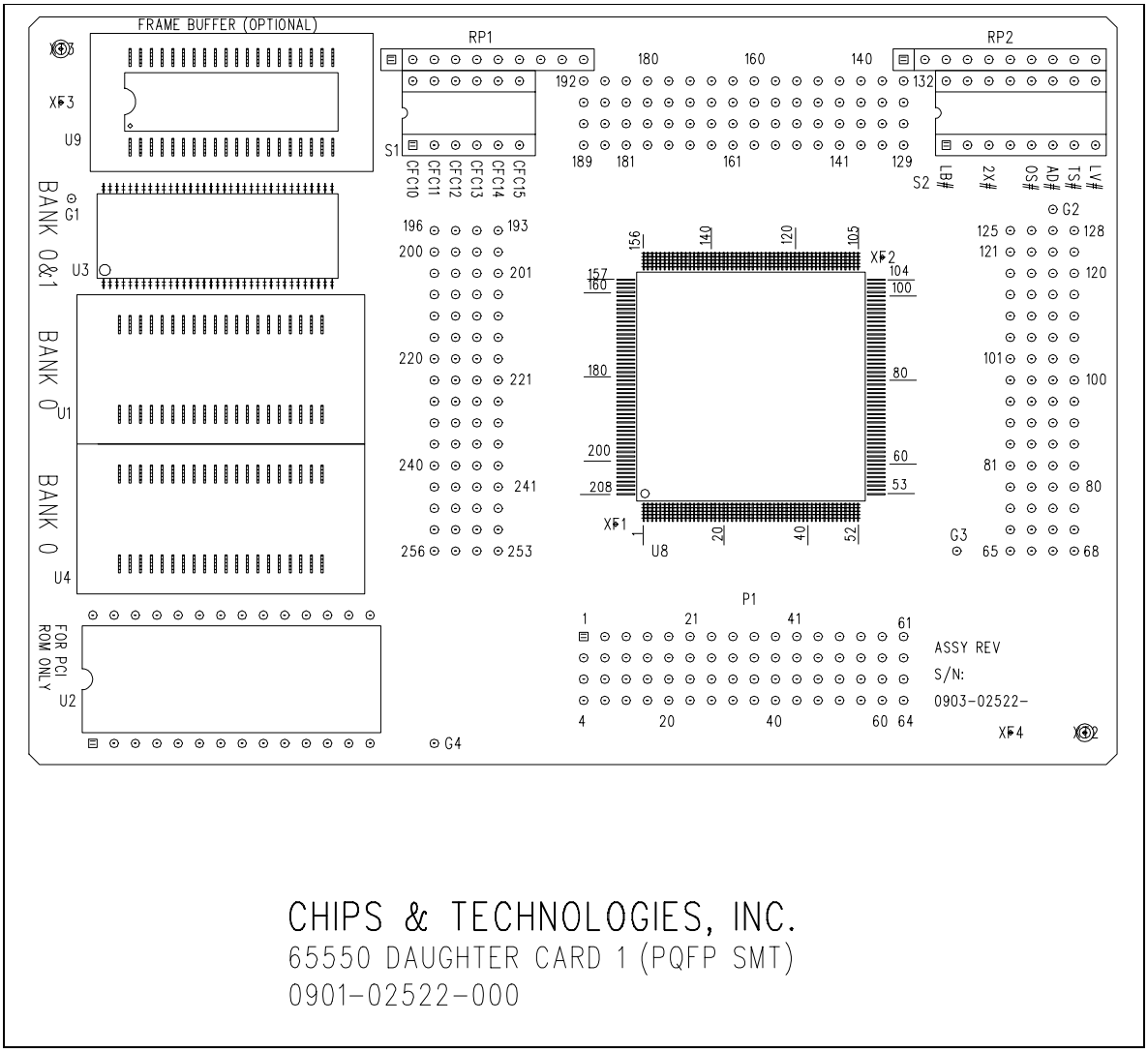

Figure 2: DK65550 Daughter Card Layout

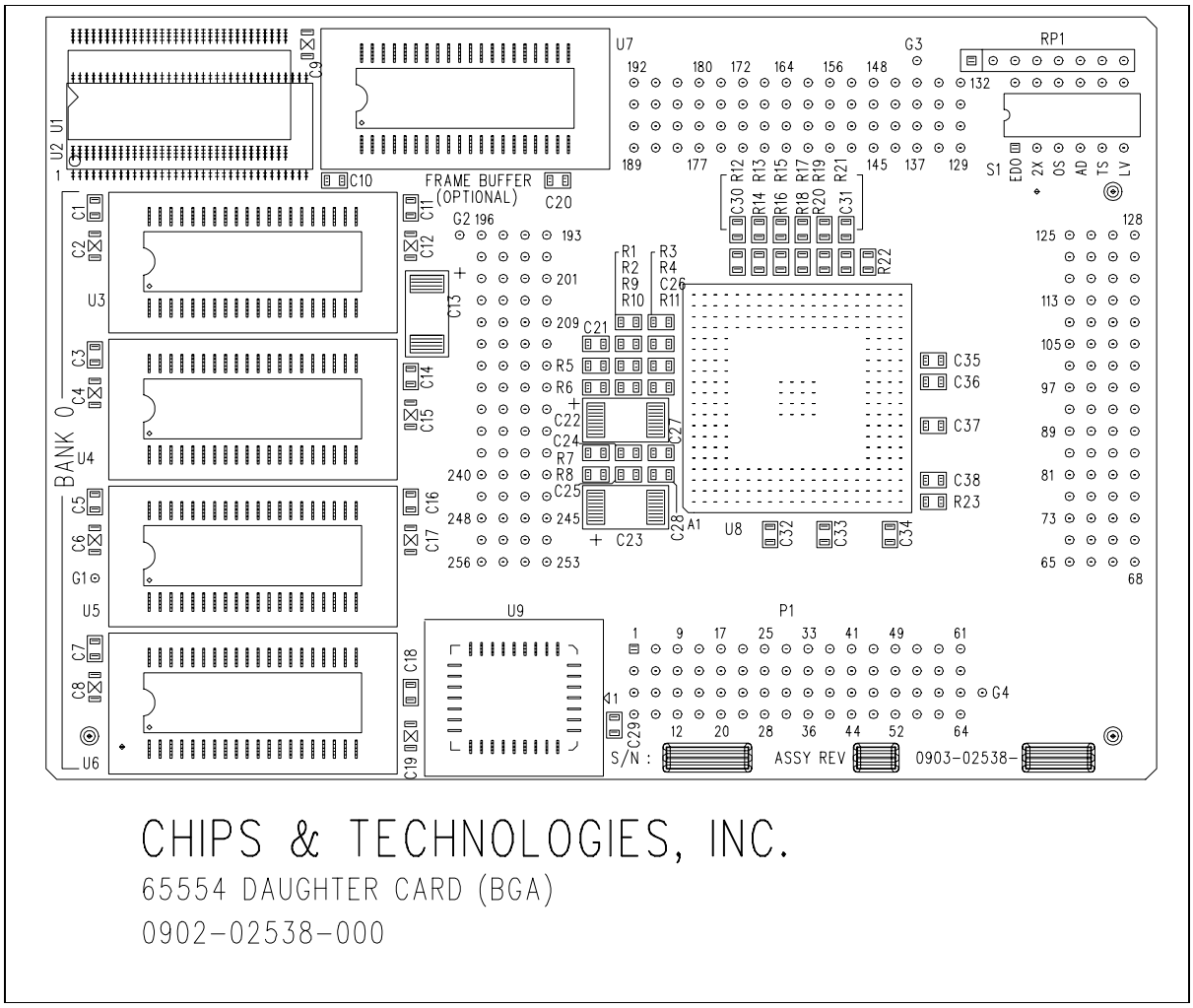

Figure 3: DK65554 Daughter Card Layout

2.1 SUMMARY OF BOARD REVISIONS

Rev B:

Limited to 24-bit panels (maximum).
Includes a VAFC connector.
Needs minor rework wires to support a 65554 daughter card.
VL-Bus version available as well as PCI version.

Rev C:

Includes 65554 support in the PCB layout.
Supports PCI Bus only.
Same as Rev B in all other respects.

Rev D:

Includes support for 36-bit panels as well as 24-bit.
VAFC connector deleted.
Improved jumpering options for GPIO pins and RGB loading.
Same as Rev C in all other respects.
All daughter cards that are usable on Rev B or Rev C are also usable on Rev D.

Rev D1:

For best TV Out picture quality, U2 pin 13 goes to analog ground rather than digital ground.
Same as Rev D in all other respects.
All daughter cards that are usable on Rev B, Rev C, or Rev D are also usable on Rev D1.

Note: Newer Rev D boards and all Rev D1 boards include rework to add a jumper for 3V panel support. This rework is described in Appendix A of the Rev D1 User's Guide (see UG156.5 dated 12/96).

Rev E:

Improved jumper options for 3.3V panel power and clean 3.3V PanelLink™ power.
Added a PCLK jumper option for PanelLink STN-DD support.
Same as Rev D1 in all other respects.
All daughter cards that are usable on Rev D1 are also usable on Rev E.

3.0 INSTALLATION

1. Unpack the DK6555X PCI board and visually inspect for any damage that may have occurred during shipping.
2. Read this User's Guide to become familiar with the board operation.
3. Check that all jumpers are in their default positions.
4. Turn off the power to the host system and plug the DK board into an available PCI slot on the motherboard. Please note that this DK board does not support ISA or VL-Bus.
5. Connect the monitor to the 15-pin VGA connector. The default configuration of the DK board is for CRT display.
6. Turn on the power and observe the sign-on message. If the sign-on message does not appear, turn off the system power and follow instructions in the troubleshooting section of this User's Guide.

4.0 CONFIGURATION SWITCHES AND JUMPERS

4.1 Power On Configurations and Daughter card

There are nine configuration bits (CFG8:0) which are latched from AA8:0 on reset. CFG7:0 are written into the HiQVideo™ controller extended register XR70[7:0], CFG8 is written into XR71[0]. The 32KHz pin can be used as CFG9 if a 32KHz input is not needed. CFG9 is latched into XR71[1] on reset.

Six additional configuration bits, CFG15:10 are latched into XR71[7:2] from MAD[7:2] on reset. The software reserves these configuration bits for input of panel IDs. They correspond to DIP switch S1 positions 6:1 on the 65550 daughter card, but the bits are not available on the DIP switches on the 65554 daughter card.

All CFG pins have internal weak pull up, and may be pulled down by 4.7k resistors on the daughter card if the DIP switches are set to **ON**. Table 1 summarizes all the CFG bits and corresponding DIP switches.

Table 1: DK6555X PCI Configuration Bits

Bits	Latched From	Name	Purpose	XR Bits	Daughter Card DIP Switch Position and Defaults	
					65550	65554
CFG0	AA0	LB#	Bus type (see Bus Type Table)	XR70[0]	S2[1]: Closed	4.7K pull down
CFG1	AA1	Reserved		XR70[1]	S2[2]: Open	—
CFG2	AA2	2X#	Bus type (see Bus Type Table)	XR70[2]	S2[3]: Open	S1[2]: Open
CFG3	AA3	Reserved		XR70[3]	S2[4]: Open	—
CFG4	AA4	Reserved		XR70[4]	—	—
CFG5	AA5	OS#	External OSC	XR70[5]	†S2[5]: Closed	S1[3]: Closed
CFG6	AA6	AD#	ENABKL & ACTI are enable	XR70[6]	S2[6]: Open	S1[4]: Open
CFG7	AA7	TS#	Internal clock test mode disable	XR70[7]	S2[7]: Open	S1[5]: Open
CFG8	AA8	LV#	Low voltage disable	XR71[0]	S2[8]: Open	S1[6]: Open
CFG10	MAD2	EDO	EDO DRAM	XR71[2]	S1[1]: Open	S1[1]: Open
CFG11	MAD3	PID0	Panel Type	XR71[3]	S1[2]: Open	—
CFG12	MAD4	PID1	Panel Type	XR71[4]	S1[3]: Open	—
CFG13	MAD5	PID2	Panel Type	XR71[5]	S1[4]: Open	—
CFG14	MAD6	PID3	Panel Type	XR71[6]	S1[5]: Open	—
CFG15	MAD7	Reserved		XR71[7]	S1[6]: Open	—

† **Note:** HiQVideo™ controller does not support internal OSC. This switch must be closed.

Although this DK board design is for PCI Bus operation, a DK board designed for the VL-Bus may also use the same 65550 daughter card. For the DK6555X-PCI board, the user should install a PCI BIOS ROM (64KB, actual code takes 32KB or 40 KB) into an EPROM socket on the daughter card. The socket should remain empty when using the DK65550-VL board. Table 2 shows the configuration bit settings for the various bus types.

The user may eliminate the need for a separate video BIOS ROM by merging and including the PCI BIOS with the system BIOS.

Table 2: DK6555X PCI Bus Type

2X# (CFG2)	LB# (CFG0)	Bus Type
LOW	LOW	Reserved
LOW	HIGH	CPU Local Bus (2X clock)
HIGH	LOW	PCI Bus (1X clock)
HIGH	HIGH	VL-Bus (not valid on this DK board or with 65554)

4.2 Push-on Jumpers

Table 3 lists the push-on jumpers supported on the DK6555X PCI board. Neither the 65550 nor 65554 daughter card has any push-on jumpers.

Table 3: DK6555X PCI Jumper Settings - (Refer to schematics for additional information)

Jumper	Setting	Description
W1	OPEN (default) CLOSED	Normal mode Standby mode
W2	OPEN CLOSED (default)	AD722 is configured as 4FSC AD722 is configured as FSC
W3	OPEN (default) CLOSED	14MHz oscillator (for 65550/65554) is enabled 14MHz oscillator is disabled
W4	1-2 (default) 2-3	External video encoder uses a dedicated 14 MHz oscillator External video encoder shares the 14MHz oscillator with 65550/65554
W5	OPEN CLOSED (default)	External video encoder is in NTSC/PAL mode External video encoder is in RGB bypass mode
W6	OPEN (default) CLOSED	External video encoder is in NTSC mode External video encoder is in PAL mode
W7	1-2 2-3 (default)	DDCDAT & DDCCLK are pulled up to DVCC55X DDCDAT & DDCCLK are pulled up to GVCC
W8	1-2 (default) 2-3	External video encoder uses CSYNC (composite sync) External video encoder uses HSYNC
W9	1-2 (default) 2-3	External video encoder uses CSYNC (composite sync) External video encoder uses HSYNC
W10	OPEN CLOSED (default)	Combined with W11, provides card present and power requirement information to system. See PCI spec for details.
W11	OPEN (default) CLOSED	See description of W10.
W12,13,14	Three 2-pin jumpers, only one of which should be closed at the same time. (Default: W14)	-VEE uses ENAVEE (W14), ENABKL (W13) or ENAVDD (W12) as power sequencing control
W15,16,17	Three 2-pin jumpers, only one of which should be closed at the same time. (Default: W15)	VDDSAFE uses ENAVEE (W17), ENABKL (W16) or ENAVDD (W15) as power sequencing control
W18,19,20	Three 2-pin jumpers, only one of which should be closed at the same time. (Default: W19)	+12VSAFE uses ENAVEE (W20), ENABKL (W19) or ENAVDD (W18) as power sequencing control

Table 3: DK6555X PCI Jumper Settings - continued (Refer to schematics for additional information)

Jumper	Setting	Description
W21	1-2	VEESAFE is -VEE
	2-3	VEESAFE is +VEE
W23	OPEN (default)	U13 regulator output (3VREG2) is clamped at 5V
	CLOSE	U13 regulator output is adjustable by pot R75 (approx 2.0-4.5V @ 1A)
W24	1-2 (default)	65550: CVCC0 & CVCC1 are W25 voltage
		65554: PVCC & SVCC are W25 voltage
	2-3	65550: CVCC0 & CVCC1 are U13 output (see W23)
		65554: PVCC & SVCC are U13 output (see W23)
W25	1-2 (default)	W25 voltage is 5V
	2-3	W25 voltage is W35 voltage
W26	1-2 (default)	OSCVCC is 5V
	2-3	OSCVCC is W35 voltage
W27	1-2 (default)	AVCC55X is 5V
	2-3	AVCC55X is W35 voltage
W28	1-2 (default)	IVCC55X is W29 voltage
	2-3	IVCC55X is output of U13 determined by W23
W29	1-2 (default)	W29 voltage is 5V
	2-3	W29 voltage is W35 voltage
W30	1-2 (default)	65550: DVCC55X is 5V
		65554: DVCC55X & CVCC55X are 5V
	2-3	65550: DVCC55X is W35 voltage
		65554: DVCC55X & CVCC55X are W35 voltage
W31	1-2 (default)	MVCC & MVCC55X are 5V
	2-3	MVCC & MVCC55X are W35 voltage
W32	1-2 (default)	BVCC55X is VIO from PCI connector (5V or 3.3v, system dependent)
	2-3	BVCC55X is W33 voltage
W33	1-2 (default)	W25 voltage is 5V
	2-3	W25 voltage is W35 voltage
W34	1-2 (default)	65550: XVCC is 5V
		65554: VVCC55X is 5V
	2-3	65550: XVCC is W35 voltage
		65554: VVCC55X is W35 voltage
W35	1-2 (default)	W35 voltage is U15 output adjustable by pot R76 (approx 2.0-5.5V @ 3A)
	2-3	W35 voltage is 3.3V from the PCI connector
W36	OPEN	For 65550 chip, header pin 63 open
	1-2	For 65554 chip, 65554 CVCC from W35 (3VMAIN)
	2-3 (default)	For 65554 chip, 65554 CVCC from GVCC (+5V), for HSYNC, VSYNC, & DDC
W37	1-2	PCLK goes to panel connector J5 instead of "M" for PanelLink STN-DD
	2-3 (default)	"M" goes to panel connector J5
W38	1-2 (default)	VDDSAFE uses GVCC (+5V)
	2-3	VDDSAFE uses 3VMAIN (W35)

Table 4: Additional DK6555X PCI Jumpers (Refer to schematics for more information)

Jumper	Settings	Description
JP1	1-2 (default)	RED output has 37.5 ohm termination on-board (for TV Out).
	OPEN	RED output has 75 ohm termination on-board (for CRT drive).
JP2	1-2 (default)	GREEN output has 37.5 ohm termination on-board (for TV Out).
	OPEN	GREEN output has 75 ohm termination on-board (for CRT drive).
JP3	1-2 (default)	BLUE output has 37.5 ohm termination on-board (for TV Out).
	OPEN	BLUE output has 75 ohm termination on-board (for CRT drive).
JP4	1-2	Panel connector J5 has DVCC55X (for LVDS interface).
	2-3	Panel connector J5 has 3VREG2 (U13) for PanelLink™ interface.
	OPEN (default)	Panel connector J5 has no additional VCC.
JP5	1-2	SCL for Multimedia daughter card is driven by JP9 pin 3.
	2-3	SDA for Multimedia daughter card is driven by JP9 pin 3.
	3-4	SDA for Multimedia daughter card is driven by ACTI/GPIO0/CSYNC.
	1-4	SCL for Multimedia daughter card is driven by ACTI/GPIO0/CSYNC.
JP6	1-2	SCL for Multimedia daughter card is driven by 54GPIO3.
	2-3	SDA for Multimedia daughter card is driven by 54GPIO3.
	3-4	SDA for Multimedia daughter card is driven by JP9/JP10 pin 1.
	1-4	SCL for Multimedia daughter card is driven by JP9/JP10 pin 1.
JP7	1-2	DDCCLK for CRT is driven by 54GPIO3.
	2-3	DDCDAT for CRT is driven by 54GPIO3.
	3-4	DDCDAT for CRT is driven by JP9/JP10 pin 1.
	1-4	DDCCLK for CRT is driven by JP9/JP10 pin 1.
JP8	1-2	DDCCLK for CRT is driven by JP9 pin 3.
	2-3	DDCDAT for CRT is driven by JP9 pin 3.
	3-4	DDCDAT for CRT is driven by ACTI/GPIO0/CSYNC.
	1-4	DDCCLK for CRT is driven by ACTI/GPIO0/CSYNC.
JP9	1-2	JP9/JP10 pin 1 is driven by 32KHZ/GPIO1/GPIO2.
	2-3	JP9 pin 3 is driven by 32KHZ/GPIO1/GPIO2.
	3-4	JP9 pin 3 is driven by ENABKL/GPIO1/CSYNC.
	1-4	JP9/JP10 pin 1 is driven by ENABKL/GPIO1/CSYNC.
JP10	1-2	JP9/JP10 pin 1 is driven by 32KHZ/GPIO1/GPIO2.
	2-3	32KHZ oscillator drives 32KHZ/GPIO1/GPIO2 signal.
	3-4	(NOT VALID)
	1-4	JP9/JP10 pin 1 is driven by 54GPIO2.
JP11	1-2	ENAVEE panel voltage control is driven by ENABKL/GPIO1/CSYNC.
	2-3	ENABKL panel control is driven by ENABKL/GPIO1/CSYNC.
	3-4	ENABKL panel control is driven by ENAVEE/ENABKL.
	1-4	ENAVEE panel voltage control is driven by ENAVEE/ENABKL.
JP12	1-2	CSYNC for TV Out is driven by ENABKL/GPIO1/CSYNC.
	2-3	Activity LED is driven by ENABKL/GPIO1/CSYNC.
	3-4	Activity LED is driven by ACTI/GPIO0/CSYNC.
	1-4	CSYNC for TV Out is driven by ACTI/GPIO0/CSYNC.
JP13	1-2	HSYNC for CRT is driven by HSYNC/CSYNC.
	2-3	CSYNC for TV Out is driven by HSYNC/CSYNC.
JP15	1-2	P34 panel data for 36-bit panels (65554 only).
	OPEN	For 65550, to avoid loading a DRAM data signal.
JP16	1-2	P35 panel data for 36-bit panels (65554 only).
	OPEN	For 65550, to avoid loading a DRAM data signal.
JP17	1-2	P32 panel data for 36-bit panels (65554 only).
	OPEN	For 65550, to avoid loading a DRAM data signal.
JP18	1-2	P30 panel data for 36-bit panels (65554 only).
	OPEN	For 65550, to avoid loading a DRAM data signal.
JP19	1-2	P33 panel data for 36-bit panels (65554 only).
	OPEN	For 65550, to avoid loading a DRAM data signal.
JP20	1-2	P31 panel data for 36-bit panels (65554 only).
	OPEN	For 65550, to avoid loading a DRAM data signal.

4.3 Multi-Function Pins

The jumper options provided by JP5 through JP13 (Table 4) allow maximum flexibility in configuring the board for virtually any desired combination of functions. Table 5 summarizes the multi-function pins available on the 65550 and 65554 and the daughter card header pins used for each function. Pin numbers preceded by "h" denote header pins between the daughter card and the DK6555X PCI board (P3). All other pin numbers refer to the individual 65550 or 65554 chip on the daughter card.

Table 5: Multi-Function Pins

Header Pin	Chip / Board	Pin	Settings	Header Pin	Chip / Board	Pin	Settings
h58	65550	53	GPIO0 / ACTI / CSYNC	h57	65550	—	Not connected
	65554	V1	GPIO0 / ACTI		65554	V3	GPIO2
h61	65550	54	GPIO1 / ENABKL / CSYNC	h60	65550	—	Not connected
	65554	U6	ENABKL		65554	U4	GPIO3
h174	65550	154	GPIO2 / 32 KHz	h72	65550	61	ENAVEE / ENABKL
	65554	T4	GPIO1 / 32KHz		65554	W4	ENAVEE / ENABKL
				h78	65550	65	HSYNC / CSYNC
					65554	U3	HYSNC / CSYNC

The GPIO numbers (e.g., GPIO 0/1/2/3), are referenced to the chip registers that control each GPIO. For example, GPIO1 is controlled by the same registers on the 65554 as on the 65550. Because of the daughter card layout, GPIO1 is routed to a different header pin on the 65554 daughter card than on the 65550 daughter card. This complicates the DK board configuration options and software compatibility. In addition, different versions of CHIPS software have attempted to correct hardware configuration problems by using different GPIO pins on the 65550 than on the 65554. Thus, boards that were configured for an older version of the software may require a different configuration for newer software versions. A recent version of the CHIPS TV multimedia daughter card software automatically detects whether the VGA controller is a 65550 or 65554. The software then adjusts the GPIO pin utilization to avoid the need for any jumper changes when changing the daughter card from 65550 to 65554 or vice versa.

In general, consult the appropriate software release notes to determine which GPIOs the software uses, and verify proper DK board setup according to the options listed above.

5.0 CONNECTORS

The table below identifies the function of the twelve different connectors on the DK6555X PCI board:

Table 6: DK Board Connector Functions

Connectors	Function
J1	SVIDEO Video connector
J2	Access Bus
J3	RCA jack, composite video out
J4	15-pin VGA connector
J5	50-pin panel connector
J7	MPEG video in connector
J8, J9, J10	Multimedia card connector
J11	P30-35 Panel data for 36-bit panels
P1, P2	PCI Bus edge connector

6.0 OPERATION

The HiQVideo™ single chip LCD/CRT controllers provide a low power, high performance, and minimal component video subsystem solution. The DK6555X PCI evaluation board is a video adapter card that implement the HiQVideo™ controllers for PCI Bus operation. The DK boards are very flexible and can support the variety of high performance and low cost options supported by the HiQVideo™ controller. The DK boards support a variety of direct panel and CRT interfaces. They provide a simple and accurate way to measure the power dissipation of various blocks of the video sub-system such as the bus interface, the video memory interface, and the display logic.

The DK boards have bus connectors with gold fingers which connect to the 32-bit PCI-Bus. The board provides the capability to evaluate all the following HiQVideo™ interfaces: bus, flat panel, CRT, memory, MPEG, multimedia card, and composite video. The boards also provide a mixed voltage capability with the ability to measure power for different blocks of the video sub-system. The minimal component video sub-system consists of the HiQVideo™ chip, and two 256Kx16 DRAMs (U1 & U4).

Refer to the 65550/65554 HiQVideo™ Data Sheets for the available resolution modes.

The user may check the power-down operation of the HiQVideo controller using a jumper (W1) on the DK board.

The DK6555X PCI board also provides features such as:

- Linear Acceleration
- DC-to-DC Conversion
- A Mixed Voltage Interface
- Power Sequencing
- Backlight Control

Although supported by the 65550 GUI accelerator, the DK6555X PCI board does not implement the VL-Bus interface or 256Kx32 DRAM configuration. Another DK board specifically designed to run the 65550 graphics controller on the VL-Bus may be used to evaluate the interface between the 65550 controller and the VL-Bus.

6.1 Bus Interface

The HiQVideo™ chip provides direct interface to 80x86 local bus. The DK boards interface with the standard 32-bit PCI Bus and supports burst mode operation. PCI is a local bus interface standard widely used in the PC industry. It provides a high performance, high integration, low cost, reliable, and flexible solution to personal computing.

6.2 Programmable Linear Acceleration

The DK6555X PCI board improves graphics performance by supporting a programmable linear addressing mode to take advantage of CHIPS 32-bit linear acceleration drivers. The programmable "Linear Acceleration" video memory provides the ability to "linearly map" the video memory to anywhere in the 32-bit system memory space in 8MB increments, thus overcoming paging and I/O bottlenecks. High performance linear acceleration drivers are available for popular application programs such as Windows™.

The user can enable or disable linear addressing using configuration bit XR0A[1]. The user can also specify the desired video buffer start address using PCI configuration register MBASE. When reset, the linear addressing mode is disabled and the base addresses of the video memory is at A000:0. See the PCI Configuration section for additional information.

6.3 Memory Interface

The daughter card contains the DRAM sockets to minimize potential noise. The user can set the display memory size through XR43[1,2] and the DRAM data bus width through XR43[4,5]. The list below shows the various possible configurations the DK6555X PCI may use when supporting the 65550 and 65554.

For 64-bit data bus (65554)

- Two 128Kx32 DRAMs (U1 & U10): bank A
- Four 256Kx16 DRAMs (U3, U4, U5 and U6): bank A
- Eight 256Kx16 DRAMs (U3, U4, U5, U6, U12, U13, U14 and U15): bank A and B
- Two 512Kx32 DRAMs (U2 & U11): bank A

For 32-bit data bus (65554)

- Two 256Kx16 DRAMs (U3 & U4): bank A
- Four 256Kx16 DRAMs (U3, U4, U12 and U13): bank A and B
- One 512Kx32 DRAM (U2): bank A

For 32-bit data bus (65550)

- Two 256Kx16 DRAMs (U1 & U4): bank A
- Four 256Kx16 DRAMs (U1, U4, U6 and U7): bank A and B
- One 512Kx32 DRAM (U3): bank A. This configuration requires rework to the daughter card. Consult the CHIPS factory for details.

Two 256Kx16 DRAMs is the minimum memory required for the DK boards. The second bank memory is optional. Two 256Kx16 DRAMs support all standard, Super VGA, and Extended VGA resolutions up to 1024x768x256 colors. The user can double the drive for all memory control and data signals by programming FR0A[4] =1.

To support the 65550, the DK6555X PCI board uses the following memory configurations:

- TWO CAS# and ONE WE# - SYMMETRIC DRAMs: XR42[4]=0
  Remove R2,R3,R6,R7,R18,R20.
  Install R1,R5,R11,R14,R21,R22.
  These components are all on the daughter card.
  This is the default configuration on the DK65550-PCI board.
- TWO WE# and ONE CAS# - SYMMETRIC DRAMs: XR42[4]=1
  Remove R1,R5,R7,R18,R20.
  Install R2,R3,R6,R11,R14,R21,R22.
  These components are all located on the daughter card.

To support the 65554, the DK6555X PCI board uses the following memory configurations:

- TWO CAS# and ONE WE# -- SYMMETRIC DRAMs: XR42[4]=0
  Remove R4, R5, R12, R15, R20
  Install R2, R9, R13, R14, R19.
  These components are all on the daughter card.
  This is the default configuration on the DK65554 board.
- TWO WE# and ONE CAS# - SYMMETRIC DRAMs: XR42[4]=1
  Remove R2, R9, R13, R14, R19.
  Install R4, R5, R12, R15, R20.
  (These components are all located on the daughter card.)

The DK6555X PCI board can support either 65550 or 65554 with EDO DRAM by configuring XR41[1-0].

6.4 Frame Buffer

LCD-DD panels require video data alternating between two separate locations in memory. In addition, a dual drive panel requires data from both locations simultaneously. These operations require a frame storage area, called a "frame buffer".

6.4.1 Embedded Frame Buffer

The HiQVideo™ controller's innovative architecture implements the frame buffer in an unused area of display memory, reducing chip count and video sub-system cost. The embedded frame buffer may be enabled by setting FR1A[0,7]=1, 0.

6.4.2 External Frame Buffer

The user may improve system performance and add more modes using LCD-DD panels by taking advantage of an external frame buffer. Both DK boards support this option using an extra 256Kx16 DRAM located on the daughter card. With external frame buffer, the display memory data bus should be 32-bit wide.

The daughter cards for the DK6555X PCI board have an SOJ socket for this external frame buffer DRAM chip. The system enables the external frame buffer by setting FR1A[0,7]=1, 1. On the 65550 daughter card, the external frame buffer does not support the PC Video and VAFC interface. The user must not enable these modes if the system uses external frame buffers. See PC Video and VAFC sections for more information. This restriction does not apply to the 65554.

To support the 65550:

The external frame buffer U9 may be either 2 WE & 1 CAS or 2 CAS & 1 WE type, 256K x 16.

- TWO CAS# and ONE WE# - SYMMETRIC DRAMs: XR42[4]=0
  Remove R24. Install R23. This is the most common configuration on the DK65550-PCI board.
- TWO WE# and ONE CAS# - SYMMETRIC DRAMs: XR42[4]=1
  Remove R23. Install R24.

To support the 65554

The external frame buffer U7 may be either 2 WE & 1 CAS or 2 CAS & 1 WE type, 256Kx16.

- TWO CAS# and ONE WE# - SYMMETRIC DRAMs: XR42[4]=0
  Remove R12. Install R13. This is the most common configuration on the DK65554 board.
- TWO WE# and ONE CAS# - SYMMETRIC DRAMs: XR42[4]=1
  Remove R13. Install R12.

6.5 Display Interface

6.5.1 Flat Panel Interface

The DK6555X PCI board has a 50-pin connector (J5) which provides all necessary signals to interface with any flat panel having a data word size of 24 bits or less. A second connector (J11) provides the 12 additional data bits needed for 36-bit panels (65554 only). The HiQVideo™ controller has enough drive for most panels and does not require any buffering on connectors J5 and J11. Tables 7 and 8 show all the pin names for different panel hook-ups. The HiQVideo™ Series controllers provide 8mA drive on all data and control signals (FR0A[2] must be set to 1 when DVCC = 3.3V). Figure 4 shows the pin assignments for the J5 connector.

	Name	Pin#	Pin#	Name
[+5V]	VDDSAFE	1	2	+12 VSAFE
(12 to 45V) or (-12V to-45V)	VEESAFE	3	4	nc or DVCC55X (see JP4)
	ENABKL	5	6	GND
	M	7	8	DE
	GND	9	10	LP
	FLM	11	12	GND
	SHFCLK	13	14	GND
	P0	15	16	P1
	GND	17	18	P2
	P3	19	20	GND
	P4	21	22	P5
	GND	23	24	P6
	P7	25	26	GND
	P8	27	28	P9
	GND	29	30	P10
	P11	31	32	GND
	P12	33	34	P13
	GND	35	36	P14
	P15	37	38	GND
	P16	39	40	P17
	GND	41	42	P18
	P19	43	44	GND
	P20	45	46	P21
	GND	47	48	P22
	P23	49	50	GND

Figure 4: DK6555X PCI Flat Panel Connector Pinout

The DK6555X PCI board supports simultaneous flat panel and CRT display. The HiQVideo™ controllers do not need an additional frame buffer for simultaneous display of CRT and single scan flat panel displays such as TFT color panels (including 24-bit), or Plasma and EL panels. For LCD-DD panels, the HiQVideo™ controllers can support simultaneous display with 60 Hz vertical refresh on both the CRT and flat panel, or with 60 Hz vertical refresh on the CRT and 120 Hz vertical refresh on the flat panel. In this mode, the ENAVEE (61), ENABKL (54), ACTI (53), M (69) and LP (68) pins have multiple functions. For detailed functions and implementations, please refer to the 65550 / 65554 Data Sheet and DK65550-PCI / DK65554 Schematics.

Pin assignments for J11 (36-bit panels) are shown in Figure 4-1 on the following page.

Name	Pin#	Pin#	Name
GND	1	2	P24
GND	3	4	P25
GND	5	6	P26
GND	7	8	P27
GND	9	10	P28
GND	11	12	P29
GND	13	14	P30
GND	15	16	P31
GND	17	18	P32
GND	19	20	P33
GND	21	22	P34
GND	23	24	P35
GND	25	26	GND

Figure 5: J11 Connector Pin Assignments

6.5.2 CRT Interface

The DK board provides direct interface to analog CRTs through an industry standard 15-pin connector J4. The DK6555X PCI board supports non-interlaced CRT monitors with resolutions up to 1024x768 with 256 colors at 75Hz. Tables 7 and 8 summarizes the HiQVideo™ pin connections for the different flat panel configurations. Refer to the 65554 data sheet for the 36-bit panel support information and 65554 pin assignments.

Table 7: 65550 Flat Panel Connection Summary

65550 Pin Information			Monochrome			Color						
Pin #	Pin Name	DK 50pin Connect.	Single Panel	DD 8 bit	DD 16-bit	TFT 16-bit	TFT 18/24-bit	TFT HR 18/24-bit	STN 4-bit Pack	STN Ext'd 4-bit Pack	STN DD 8-bit	STN DD 16-bit
Pixels Transferred Per Shift Clock --->			8	8	16	1	1	2	5-1/3	2-2/3	2-2/3	5-1/3
71	P0	15	–	UD3	UD7	B0	B0	B00	R0...	R0...	UR0...	UR0...
72	P1	16	–	UD2	UD6	B1	B1	B01	G0...	B0...	UG0...	UG0...
73	P2	18	–	UD1	UD5	B2	B2	B02	B0...	G1...	UB0...	UB0...
74	P3	19	–	UD0	UD4	B3	B3	B03	R1...	R2...	UR1...	UR1...
75	P4	21	–	LD3	UD3	B4	B4	B10	G1...	B2...	LR0...	LR0...
76	P5	22	–	LD2	UD2	G0	B5	B11	B1...	G3...	LG0...	LG0...
78	P6	24	–	LD1	UD1	G1	B6	B12	R2...	R4...	LB0...	LB0...
79	P7	25	–	LD0	UD0	G2	B7	B13	G2...	B4...	LR1...	LR1...
81	P8	27	P0	–	LD7	G3	G0	G00	B2...	SHFCLKU	–	UG1...
82	P9	28	P2	–	LD6	G4	G1	G01	R3...	–	–	UB1...
83	P10	30	P3	–	LD5	G5	G2	G02	G3...	–	–	UR2...
84	P11	31	P4	–	LD4	R0	G3	G03	B3...	–	–	UG2...
85	P12	33	P5	–	LD3	R1	G4	G10	R4...	–	–	LG1...
86	P13	34	P6	–	LD2	R2	G5	G11	G4...	–	–	LB1...
87	P14	36	P7	–	LD1	R3	G6	G12	B4...	–	–	LR2...
88	P15	37	–	–	LD0	R4	G7	G13	R5...	–	–	LG2...
90	P16	39	–	–	–	–	R0	R00	–	–	–	–
91	P17	40	–	–	–	–	R1	R01	–	–	–	–
92	P18	42	–	–	–	–	R2	R02	–	–	–	–
93	P19	43	–	–	–	–	R3	R03	–	–	–	–
94	P20	45	–	–	–	–	R4	R10	–	–	–	–
95	P21	46	–	–	–	–	R5	R11	–	–	–	–
96	P22	48	–	–	–	–	R6	R12	–	–	–	–
97	P23	49	–	–	–	–	R7	R13	–	–	–	–
54/61	ENABKL	5	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL
70	SHFCLK	13	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLKL	SHFCLK	SHFCLK
69	M	7	M	M	M	M	M	M	M	M	M	M
68	LP	10	LP	LP	LP	LP	LP	LP	LP	LP	LP	LP
67	FLM	11	FLM	FLM	FLM	FLM	FLM	FLM	FLM	FLM	FLM	FLM
68/69	DE	8	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE
–	VDDSAFE	1	–	–	–	–	–	–	–	–	–	–
–	+12VSAFE	2	–	–	–	–	–	–	–	–	–	–
–	VEESAFE	3	–	–	–	–	–	–	–	–	–	–
–	GND	6,9,12,14, 17,20,23, 26,29,32, 35,38,41, 44,47,50	–	–	–	–	–	–	–	–	–	–

Table 8: 65554 Flat Panel Connection Summary

65554 Pin Information			Monochrome			Color						
Pin #	Pin Name	DK 50pin Connect.	Single Panel	DD 8 bit	DD 16-bit	TFT 16-bit	TFT 18/24-bit	TFT HR 18/24-bit	STN 4-bit Pack	STN Extended 4-bit Pack	STN DD 8-bit	STN DD 16-bit
Pixels Transferred Per Shift Clock --->			8	8	16	1	1	2	5-1/3	2-2/3	2-2/3	5-1/3
W6	P0	15	–	UD3	UD7	B0	B0	B00	R0...	R0...	UR0...	UR0...
V7	P1	16	–	UD2	UD6	B1	B1	B01	G0...	B0...	UG0...	UG0...
Y6	P2	18	–	UD1	UD5	B2	B2	B02	B0...	G1...	UB0...	UB0...
W7	P3	19	–	UD0	UD4	B3	B3	B03	R1...	R2...	UR1...	UR1...
V8	P4	21	–	LD3	UD3	B4	B4	B10	G1...	B2...	LR0...	LR0...
V7	P5	22	–	LD2	UD2	G0	B5	B11	B1...	G3...	LG0...	LG0...
W8	P6	24	–	LD1	UD1	G1	B6	B12	R2...	R4...	LB0...	LB0...
U9	P7	25	–	LD0	UD0	G2	B7	B13	G2...	B4...	LR1...	LR1...
V9	P8	27	P0	–	LD7	G3	G0	G00	B2...	SHFCLKU	–	UG1...
Y8	P9	28	P2	–	LD6	G4	G1	G01	R3...	–	–	UB1...
W9	P10	30	P3	–	LD5	G5	G2	G02	G3...	–	–	UR2...
Y9	P11	31	P4	–	LD4	R0	G3	G03	B3...	–	–	UG2...
V10	P12	33	P5	–	LD3	R1	G4	G10	R4...	–	–	LG1...
W10	P13	34	P6	–	LD2	R2	G5	G11	G4...	–	–	LB1...
Y10	P14	36	P7	–	LD1	R3	G6	G12	B4...	–	–	LR2...
U10	P15	37	–	–	LD0	R4	G7	G13	R5...	–	–	LG2...
U11	P16	39	–	–	–	–	R0	R00	–	–	–	–
W11	P17	40	–	–	–	–	R1	R01	–	–	–	–
Y11	P18	42	–	–	–	–	R2	R02	–	–	–	–
V11	P19	43	–	–	–	–	R3	R03	–	–	–	–
Y12	P20	45	–	–	–	–	R4	R10	–	–	–	–
Y13	P21	46	–	–	–	–	R5	R11	–	–	–	–
V12	P22	48	–	–	–	–	R6	R12	–	–	–	–
U12	P23	49	–	–	–	–	R7	R13	–	–	–	–
U6	ENABKL	5	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL
Y5	SHFCLK	13	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLKL	SHFCLK	SHFCLK
V6	M	7	M	M	M	M	M	M	M	M	M	M
Y4	LP	10	LP	LP	LP	LP	LP	LP	LP	LP	LP	LP
W5	FLM	11	FLM	FLM	FLM	FLM	FLM	FLM	FLM	FLM	FLM	FLM
Y4/V6	DE	8	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE
–	VDDSAFE	1	–	–	–	–	–	–	–	–	–	–
–	+12VSAFE	2	–	–	–	–	–	–	–	–	–	–
–	VEESAFE	3	–	–	–	–	–	–	–	–	–	–
_	GND	6,9,12,14, 17,20,23, 26,29,32, 35,38,41, 44,47,50	_	_	_	_	_	_	_	_	_	_

6.6 Clock

6.6.1 14MHz Reference Clock

The 65550 controller uses a TTL 14MHz signal connected to pin 203 as the reference clock, while the 65554 controller uses the signal connected to pin C3. This clock provides a timing reference to all the internal logic blocks such as sequencer, CRT controller, and graphics controller.

6.6.2 32KHz Clock

Panel power sequencing also requires a reference clock. Pin 154 supplies the 65550 chip (Pin T4 on the 65554 chip) with a 32KHz signal for this purpose. This clock also refreshes the DRAM. If the system uses non-self-refresh DRAMs, do not apply this external 32KHz clock to the chip (Y2 is not stuffed). This configuration generates a 37.3KHz signal from the internal 14MHz power sequencing clock. Please refer to the XRCF[3] definition in the data sheet for details.

6.7 Utilities and Drivers

The SETCLK utility included in the utilities diskette independently programs MCLK and DCLK of the HiQVideo™ controller. The diskette also provides other utilities such as 55xDEBUG and MODETEST. The 55xDEGUB is a debug program that facilitates reading and writing HiQVideo registers to enable or disable features. The MODETEST utility runs through all the standard VGA modes and super VGA modes. More detailed information is available in file 55xDEMO.DOC on the DEMO/UTILITY distribution disk. The driver diskettes also contain high performance display drivers for Windows, AutoCAD, LOTUS 1-2-3, WordPerfect, and so on for your evaluation. The diskettes contain text files to help you install of these drivers.

6.8 PCI Configuration

The PCI definition provides for complete software driven initialization and configuration using a separate configuration address space. PCI devices may use 256 bytes of configuration address space for this purpose. For the PCI Bus configuration, the HiQVideo™ controllers use ten registers to identify the chip, examine the various internal states, configure the video memory and BIOS ROM base address, and control of settings for the various operating modes. These registers are located in the PCI configuration space. The HiQVideo™ controllers supports both I/O mapped memory, and memory mapped I/O.

6.9 BIOS Interface

Both the DK6555X PCI incorporates a PCI Video BIOS in a 27C512 EPROM (U2 on 65550 daughter card and U9 on the 65554 daughter card. The code size is 32KB (or 40KB) resident at address 0C0000. The HiQVideo™ controller generates the ROMCS# signal for the BIOS ROM. The 65550 and 65554 PCI BIOS is developed for use with PCI local bus configuration as defined in the PCI Local Bus Specification Rev. 2.0. Each BIOS uses word pointers to the PCI Data Structure at offset C000:18/E000:18. Table 8 defines the PCI data structure.

Table 9: PCI Data Structure

Register Mnemonic	Register Name	Offset
VENID	Vendor ID	00h
DEVID	Device ID	02h
DEVCTL	Device Control	04h
DEVSTAT	Device Status	06h
REV	Revision ID	08h
PRG	Programming Interface	09h
SUB	Sub Class Code	0Ah
BASE	Base Class Code	0Bh
MBASE	Memory Base Address	10h
RBASE	ROM Base Address	30h

Note: The PCI BIOS is usually included in and merged with the system BIOS. For more detailed information, please refer to the 65550/65554 data sheet and the 65550/65554 VGA BIOS OEM Reference Guide.

6.10 VAFC Interface

Although the 65550 and 65554 support a limited VAFC interface, the DK6555X PCI board does not provide connector support specifically for VAFC. Most of the necessary signals are available on the MPEG and Multimedia connectors, J7 through J10.

6.11 PC Video Interface

The HiQVideo™ graphics controller provides an interface to CHIPS PC Video: 69001A (82C9001A) and 69003/4 video windowing controllers to display *LIVE* video on flat panel or CRT displays. The user can use XR60, XRD0, and MR3C to enable and disable an 18-bit PC Video interface. Since the PC Video interface does not support the external frame buffer, the user must physically remove the frame buffers before enabling the PC Video.

The DK6555X PCI board does not provide connectors specifically for PC Video interface, but most of the necessary signals are available on the MPEG and Multimedia connectors, J7 through J10.

6.12 NTSC/PAL Composite Video Output (TV Out)

The HiQVideo™ controllers provide video encoder support and a composite sync signal which some video encoders require. DK boards incorporate an NTSC/PAL encoder from Analog Device (AD722 or AD723) to convert the VGA signals to the composite NTSC video and S-VHS video signals. The board provides a composite NTSC video connector J3 and a S-VHS video connector J1. Pins W5 and W6 switch between NTSC and PAL modes.

Composite Video Output is also referred to as TV Out. It can be either NTSC or PAL format.

6.13 Multimedia Card Interface

The DK6555X PCI board provides a video interface from a multimedia card or zoom video port (ZV port). The 65550 MM card provides YUV video to the DK board For more detailed information, please refer to the MM6555x MM card user's guide. Figure 5 shows the multimedia connector pinouts.

J8

Name	Pin#	Pin#	Name
GND	1	2	Y0
GND	3	4	Y1
GND	5	6	Y2
GND	7	8	Y3
GND	9	10	Y4
GND	11	12	Y5
GND	13	14	Y6
GND	15	16	Y7
GND	17	18	HREF
GND	19	20	VREF
GND	21	22	LLC2
GND	23	24	GND
GND	25	26	NC

J10

Name	Pin#	Pin#	Name
GND	1	2	UV0
GND	3	4	UV1
GND	5	6	UV2
GND	7	8	UV3
GND	9	10	UV4
GND	11	12	UV5
GND	13	14	UV6
GND	15	16	UV7
GND	17	18	SDA
GND	19	20	SCL
GND	21	22	NC
GND	23	24	NC
GND	25	26	NC

J9

NAME	PIN#	PIN#	NAME
GND	1	2	+5V
GND	3	4	+5V
GND	5	6	+12V
GND	7	8	+12V
GND	9	10	-12V
C-GND	11	12	-12V

Figure 6: Multimedia Connector Pinout

6.14 MPEG and ZV Video In Connector

The DK65550X PCI also provides another connector for YUV video interface. The J7 connector receives YUV data from an MPEG or PCMCIA ZV interface card. Figure 6 shows pinout.

NAME	PIN#	PIN#	NAME
GND	1	2	Y0
GND	3	4	Y1
GND	5	6	Y2
GND	7	8	Y3
GND	9	10	Y4
GND	11	12	Y5
GND	13	14	Y6
GND	15	16	Y7
GND	17	18	UV0
GND	19	20	UV1
GND	21	22	UV2
GND	23	24	UV3
GND	25	26	UV4
GND	27	28	UV5
GND	29	30	UV6
GND	31	32	UV7
GND	33	34	HREF
GND	35	36	VREF
GND	37	38	LLC2
GND	39	40	GND

Figure 7: MPEG Video In Connector

6.15 Activity Indicator

The HiQVideo™ controller provides an output pin called ACTI (65550 pin 53, 65554 pin V1) to facilitate an orderly power-down sequence. The ACTI output is an active high signal which is driven high every time the CPU executes a valid VGA memory read/write operation or VGA I/O read/write operation. The DK6555X PCI board has an LED (D7) on the ACTI pin, which will glow whenever there is a VGA access. This pin is configured as Activity Indicator by default when FR0C[4:3]=00. The power management logic may use this signal to put the HiQVideo™ controller into Panel Off or Standby power-down modes.

6.16 Mixed Voltage Generation and Power Measurement

The DK6555X PCI board has jumpers to choose different supply voltages for each block of the video sub-system. The voltages chosen could be 5V from the bus, 3.3V from the bus, or a voltage from an on-board voltage regulator. The latter voltage is adjustable by resistor pots, except for the internal clock power supply. All HiQVideo™ controller interfaces can be run at either +5V or +3.3V independent of each other. To support the 65550, CVCC (CVCC0 & CVCC1) must follow the internal core logic voltage IVCC55X. To support the 65554, PVCC & SVCC must follow the internal core logic voltage IVCC55X. In addition, HiQVideo™ controllers provide an easy and accurate way to measure the power dissipation of the various blocks of the video subsystem.

Table 9 describes the various blocks of the video sub-system supplied by individually configurable voltages, as well as where to measure these voltages and the power dissipation (current) for each block. For information on how to configure them to 5V or 3.3v, refer to the Jumper Set-up Table or the DK board schematics.

Table 10: Video Sub-System Voltages

DK6555X Voltage Name	Blocks of Video Sub-system Supplied by the Voltage	Voltage Measurement Point	Current Measurement Point
GVCC	BIOS, Video encoder digital Vcc	W34 pin 1	SH5
AVCC	Video encoder analog Vcc	W34 pin 1	FB10
XVCC55X	Video capture port	W34 pin 2	W34
BVCC55X	Bus interface	W32 pin 2	W32
MVCC	DRAMs and external frame buffer	W31 pin 2	SH2
MVCC55X	Memory logic	W31 pin 2	SH1
DVCC55X	Display interface	W30 pin 2	W30
IVCC55X	65550/65554 internal logic	W28 pin 2	W28
AVCC55X	Internal DAC	W27 pin 2	W27
OSCVCC	External oscillator	W26 pin 2	W26

For 65550 Only Voltage name	Blocks of Video Sub-system Supplied by the Voltage	Voltage Measurement Point	Current Measurement Point
CVCC0	Internal clock synthesizer power 0	W24 pin 2	SH7
CVCC1	Internal clock synthesizer power 1	W24 pin 2	SH6

For 65554 Only Voltage Name	Blocks of Video Sub-system Supplied by the Voltage	Voltage Measurement Point	Current Measurement Point
VVCC55X	Video interface	W34 pin 2	W34
CVCC55X	CRT interface	W36 pin 2	W36
PVCC	Internal clock synthesizer power 0	W24 pin 2	SH7
SVCC	Internal clock synthesizer power 1	W24 pin 2	SH6

Example: To measure the power consumed by the internal DAC of the 65554, replace the W27 jumper plug with an ammeter. The desired voltage may be measured at W27 pin 2.

6.17 Power Sequencing and Backlight Control

Flat panel displays are extremely sensitive to conditions where full biasing voltage VEESAFE is applied to the liquid crystal material without enabling the control and data signals to the panel.

The DK6555X PCI board provides three controlled panel voltages: VDDSAFE (VDD) for driver electronics, VEESAFE (VEE) for LCD bias, and +12VSAFE (BACKLIGHT) for easy access for most panels. The power sequencing control output signals ENAVEE, ENAVDD, and ENABKL regulate application of bias voltage and +5V to the panel and +12 V to the inverter for backlight operation.

6.18 DC-to-DC Converter

The DK board has an on-board DC-to-DC converter to provide easy access to the controlled DC voltage (LCD bias voltage) for most panels. The voltage range is -12 to -45VDC (Negative) OR +12 to +45VDC (Positive). To receive a (-VEE) voltage in the range of -12 to -45Volts, adjust resistor pot R59. Measure the voltage at W21 Terminal 1. Place a jumper on W21(1-2). To get a positive (+VEE) voltage in the range of +12 to +45Volts, adjust the resistor pot R59 and measure the voltage at W21 Terminal 3. Place a jumper on W21 (2-3). Remove power from the system. Hook up the panel to the panel connectors. Turn on the power. This may lower the voltage at W21 because of the voltage drop caused by the panel load. Adjust pot R59 again for proper panel voltage. The voltage VEESAFE at W21 (+VEE or -VEE) may be generated by the formula:

$$R64 = (R66+R59) * \{(VEESAFE \div 1.31) - 1\}$$

WARNING: Improper use of the DC-to-DC Converter may cause damage to the panel.

6.19 PanelLink™ & LVDS Interfaces

The DK board allows a PanelLink™ or LVDS transmitter adapter card to be installed in the panel connector, J5. Various jumper options allow flexible selection of 3.3V or 5V power for the adapter card, as well as a PCLK option for STN-DD panel support via a PanelLink or LVDS interface.

A) PCLK for PanelLink™ STN-DD support

If the PanelLink interface is operated at 3.3V as described below, then there may be a problem with the PCLK voltage level. Ideally, PCLK should be reduced to 3.3V, but this may not be feasible because of the video capture port VCC requirements. (With either a 65554 or 65550 daughter card, XVCC55X on the main DK board provides the VCC power for the video capture port as well as PCLK.) A possible solution for PCLK may be to add a 1KΩ resistor in series with PCLK as close to the PanelLink clock input as possible, to limit the current that might otherwise flow when a 5V PCLK signal drives a 3.3V PanelLink clock input. This solution has not yet been characterized or tested. The PCLK voltage level is not an issue when using a TFT panel since SHFCLK is used for the PanelLink clock in that case.

B) Clean 3.3V power for the PanelLink transmitter.

JP4 allows 3.3V to be supplied to the PanelLink transmitter and receiver cards from the 3V regulator U13 (voltage adjusted by R75). JP4 also allows 5V to be used instead, for other types of interfaces such as 5V LVDS. For PanelLink operation, only the PanelLink transmitter and receiver cards should be powered from this regulator (via JP4), and the voltage should be set to 3.3V (within 5%). In addition, the DVCC55X voltage should also be set for 3.3V, from U15 via W35 and W30. Any other 3.3V voltages used in the system (except for the PanelLink interface) should also come from the U15 regulator. The reason for separating the PanelLink voltage from the other 3.3V loads is to provide a very clean 3.3V source to the PanelLink chips. This is most important at XGA frequencies (65 MHz).

The Rev E DK board, unlike earlier revisions, has an improved W36 jumper to allow 65554 CVCC to remain at 5V when DVCC55X is set to 3.3V. This allows the CRT interface (HSYNC, VSYNC, and GPIO pins for DDC support) to operate at 5V if needed, independently of DVCC55X. This option is not available when using a 65550 daughter card. The 65550 chip itself uses DVCC for CRT signals as well as panel signals, so there is no way to separate the voltages externally. Most CRTs probably will operate satisfactorily, since the 3.3V levels are still TTL-compatible. However, when using a 65550 daughter card, JP5 through JP8 should remain open to prevent any possibility of driving 5V levels into the 65550 from the DDCDAT or SDA signals. Again, the DDCDAT/SDA issue only applies when using a 65550 daughter card. The 65554 chip and daughter card (and follow-on products) do not have this restriction.

It is acceptable to switch IVCC, AVCC, and other 65550/65554 voltages to 3.3V if desired, as long as they are operated from the U15 regulator (W35 jumper). The next section provides a comprehensive example listing of DK Board jumper settings for using the Generic PanelLink card set.

C) Configuration Example

Application: DK6555X PCI Board, Rev E, with 65554 daughter card, for use with a Generic PanelLink™ Card set driving a TFT panel.

Table B-1: Jumpers Underneath the 65554 Daughter Card

Jumper	Function*	State**
W1	sh.2, STANDBY	off
W2	sh.5, TV Out	off
W3	sh.2, 14 MHz	off
W4	sh.5, TV Out	1-2
W5	sh.5, TV Out	on
W6	sh.5, TV Out	off
W7	sh.5, DDC Pull Up	2-3
W8	sh.5, TV Out	2-3
W9	sh.5, TV Out	2-3
W10	sh.3, PCI	on
W11	sh.3, PCI	off
JP1	sh.5, TV Out	off
JP2	sh.5, TV Out	off
JP3	sh.5, TV Out	off
JP5	sh.2, I2C	all off
JP6	sh.2, I2C	all off
JP7	sh.2, DDC	1-2 & 3-4
JP8	sh.2, DDC	all off
JP9	sh.2, GPIO	all off
JP10	sh.2, GPIO	1-4 & 2-3
JP11	sh.2, GPIO	1-4 & 2-3
JP12	sh.2, GPIO	1-4
JP13	sh.2, HSYNC	1-2
JP15	sh.2, P34	on
JP16	sh.2, P35	on
JP17	sh.2, P32	on
JP18	sh.2, P30	on
JP19	sh.2, P33	on
JP20	sh.2, P31	on

Table B-2: Jumpers & Pots <u>not</u> Underneath the Daughter Card

Jumper	Function*	State**
JP4	sh.5, PanelLink VCC	2-3
W12	sh.5, VEESAFE	off
W13	sh.5, VEESAFE	off
W14	sh.5, VEESAFE	on
W15	sh.5, VDDSAFE	on
W16	sh.5, VDDSAFE	off
W17	sh.5, VDDSAFE	off
W18	sh.5, +12SAFE	off
W19	sh.5, +12SAFE	on
W20	sh.5, +12SAFE	off
W21	sh.5, VEESAFE	all off
W23	sh.4, 3VREG2	on
W24	sh.4, CVCC0	1-2
W25	sh.4, CVCC0/1	1 -2
W26	sh.4, OSCVCC	1 -2
W27	sh.4, AVCC55X	1 -2
W28	sh.4, IVCC55X	1 -2
W29	sh.4, IVCC55X	1 -2
W30	sh.4, DVCC55X	2-3
W31	sh.4, MVCC/55X	1 -2
W32	sh.4, BVCC55X	1 -2
W33	sh.4, BVCC55X	1 -2
W34	sh.4, XVCC55X	2-3
W35	sh.4, 3VMAIN)	1 -2
W36	sh.2, 65554 CVCC	2-3
W37	sh.5, M/PCLK	2-3
W38	sh.5, Panel VCC	1 -2
R59	sh.5, VEESAFE	Note (1)
R75	sh.4, 3VREG2	Note (2)
R76	sh.4, 3VMAIN	Note (3)

Notes:

1) Set for panel requirement
2) Set for 3.3V on W24 pin 3
3) Set for 3.3V on W25 pin 3

* Schematic reference and functional category.

** "on" – Jumper plug is installed
"off" – Jumper plug is not installed

6.20 Configuration Example for 65555

Application: DK6555X PCI Board, Rev E, with 65555 HiQVideo™ controller mounted on a 65554 daughter card. 3.3V DRAM, TV Out enabled, not using a PanelLink™ interface.

Important: The 65555 requires 3.3V on all of its VCC pins, but is 5V tolerant on signal inputs and tri-stated outputs. Output pins clamp at 3.3V or GND when driving high or low, respectively, but can tolerate a pull-up resistor to +5V as long as the resistor limits the current into the 65555 output pin to within the 65555 DC specifications.

Table B-1: Jumpers Underneath the 65554 Daughter Card

Jumper	Function*	State**
W1	sh.2, STANDBY	off
W2	sh.5, TV Out	off
W3	sh.2, 14 MHz	off
W4	sh.5, TV Out	1-2
W5	sh.5, TV Out	off
W6	sh.5, TV Out	off
W7	sh.5, DDC Pull Up	2-3
W8	sh.5, TV Out	1-2
W9	sh.5, TV Out	2-3
W10	sh.3, PCI	on
W11	sh.3, PCI	off
JP1	sh.5, TV Out	on
JP2	sh.5, TV Out	on
JP3	sh.5, TV Out	on
JP5	sh.2, I2C	all off
JP6	sh.2, I2C	all off
JP7	sh.2, DDC	1-2 & 3-4
JP8	sh.2, DDC	all off
JP9	sh.2, GPIO	all off
JP10	sh.2, GPIO	1-4 & 2-3
JP11	sh.2, GPIO	1-4 & 2-3
JP12	sh.2, GPIO	3-4
JP13	sh.2, HSYNC	1-2
JP15	sh.2, P34	on
JP16	sh.2, P35	on
JP17	sh.2, P32	on
JP18	sh.2, P30	on
JP19	sh.2, P33	on
JP20	sh.2, P31	on

Notes:

* Schematic reference and functional category.

** "on" – Jumper plug is installed
"off" – Jumper plug is not installed

1) Set for panel requirement
2) Set for 3.3V on W24 pin 3
3) Set for 3.3V on W25 pin 3

Table B-2: Jumpers & Pots not Underneath the Daughter Card

Jumper	Function*	State**
JP4	sh.5, Panel VCC	all off
W12	sh.5, VEESAFE	off
W13	sh.5, VEESAFE	off
W14	sh.5, VEESAFE	on
W15	sh.5, VDDSAFE	on
W16	sh.5, VDDSAFE	off
W17	sh.5, VDDSAFE	off
W18	sh.5, +12SAFE	off
W19	sh.5, +12SAFE	on
W20	sh.5, +12SAFE	off
W21	sh.5, VEESAFE	all off
W23	sh.4, 3VREG2	on
W24	sh.4, CVCC0	2-3
W25	sh.4, CVCC0/1	2-3
W26	sh.4, OSCVCC	2-3
W27	sh.4, AVCC55X	2-3
W28	sh.4, IVCC55X	2-3
W29	sh.4, IVCC55X	2-3
W30	sh.4, DVCC55X	2-3
W31	sh.4, MVCC/55X	2-3
W32	sh.4, BVCC55X	2-3
W33	sh.4, BVCC55X	2-3
W34	sh.4, XVCC55X	2-3
W35	sh.4, 3VMAIN)	1 -2
W36	sh.2, 65555 CVCC	1-2
W37	sh.5, M/PCLK	2-3
W38	sh.5, Panel VCC	2-3
R59	sh.5, VEESAFE	Note (1)
R75	sh.4, 3VREG2	Note (2)
R76	sh.4, 3VMAIN	Note (3)

On the daughter card, set the following S1 switches:
Positions 1, 3, and 6 to "ON".
Positions 2, 4, and 5 to "OFF".

7.0 TROUBLESHOOTING

1. Check that all jumpers and DIP switch positions are set to their default positions.
2. Verify that socket U2 on the 65550 daughter card (or U9 on the 65554 daughter card) contains a PCI BIOS ROM.
3. Verify that the other parts in the system function properly by using a known working VGA board with the system.
4. If the DK6555X PCI board still does not work, contact your CHIPS representative.

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